NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

IN-SITU TESTING OF RADIATION EFFECTS ON VLSI CAPACITORS USING THE NPS LINEAR ACCELERATOR

by

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December 1996

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REPORT DOCUMENTATION PAGE

Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE December 1996	3. REPORT TYPE AND DATES COVERED Master's Thesis

4. TITLE AND SUBTITLE
IN-SITU TESTING OF RADIATION EFFECTS ON VLSI CAPACITORS USING THE NPS LINEAR ACCELERATOR

5. FUNDING NUMBERS

6. AUTHOR(S)
Salsbury, Duane

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Naval Postgraduate School
Monterey CA 93943-5000

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(maximum 200 words)*

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14. SUBJECT TERMS Radiation Effects on Electronic Devices, Total Dose Radiation Effects, Naval Postgraduate School	15. NUMBER OF PAGES 110
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT UL

NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18

98-102

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IN-SITU TESTING OF RADIATION EFFECTS ON VLSI CAPACITORS USING THE NPS LINEAR ACCELERATOR

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Submitted in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
December 1996

ABSTRACT

The study of radiation effects on VLSI components is a very heavily researched topic. There are several reasons for this research, one of which is the application of VLSI components to space related vehicles. One component essential to Analog VLSI elements is the capacitor. The purpose of this paper is to better define the actual effects of radiation on the MOS VLSI capacitor. The radiation testing is conducted using the NPS electron linear accelerator. The data is taken while the capacitor is being exposed to an accumulating dose of electron radiation. The capacitance values are monitored using the parameter changes of a specially designed low pass filter circuit. The 3 dB breakpoint frequency of this filter is used to calculate the actual capacitance. The capacitance value is then related to the accumulated radiation dose in Rads. The results are very important and needed, especially if off-the-shelf components are to be utilized in the design of spacecraft systems.

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ACKNOWLEDGMENTS

I would like to acknowledge several people for their help and support on this project. First, my wife Patty whose patience and perseverance really got me through when I was more then a little discouraged. I would also like to thank my five children; Claressa, Benjamin, Aaron, Amanda and Joel for their patience and long-suffering while Dad was busy with his thesis. Thanks to Dr. Sherif Michael for taking the time to be my advisor. A huge thanks goes to the Linear Accelerator staff, Don Snyder and Harold Rietdyk, as this experiment would not have been possible without their hard work in repairing and operating the LINAC as well as their exhaustive knowledge of the LINAC operations. Also, I would like to thank the Space Systems Academic Group PANSAT design team for the use of their digital camera.

I. INTRODUCTION

A. OVERVIEW

The primary research question covered by this thesis is, how MOS VLSI capacitors respond in a radiation flux. This question has been asked before. As an answer there exist published results regarding this question (Winokur, 1984) (Benedetto, 1984). Some of these results are discussed in this paper. What has not been done, except here at The Naval Postgraduate School, is collecting the data while the chips containing the capacitors are being irradiated. This in-situ testing was first conceived by Professor Sherif Michael in 1989 in the testing of Op-Amps. In 1995 it was used by one of his thesis students Stuart Abrahamson to test capacitors (Abrahamson, 1995). The method of in-situ radiation testing of VLSI chips is discussed in Chapter V.

The next question is, why does this primary question need answered? Or, why does one care about the effects of radiation on VLSI circuitry? To answer this, one has to go back in time to the 1950's and 1960's. Space exploration was just beginning to take off. The United States and the Soviet Union were in a huge race to see who could out do the other in space exploration. In addition to exploring space, or at least the upper atmosphere, the US and the USSR conducted some exoatmospheric nuclear tests. The most notable by the US was the Starfish test conducted off Johnson Island in the Pacific ocean. The test took place on 9 July, 1958 at an altitude of 400 km (248.5 miles). The yield of the blast was 1400 kilotons. That same year the USSR conducted similar tests with yields in the hundreds of kilotons. These tests caused a significant disruption in the radiation belts surrounding the earth (see Chapter II). They actually caused the Telstar I,

an orbiting communications satellite, to fail. This got the attention of the United States and prompted a great deal of research in the area of space radiation environments. (Tabbert, 1993, pp. 2.1-2)

Once there was a reasonable understanding of the space environment, research began on how to build satellites that could exist in these harsh surroundings. During this time (late 50's to early 70's) great progress was made in the area of transistors and integrated circuits (IC's). The use of IC's in space was a perfect match. They were small compact and provided the satellite designer with a great deal of computing power. They used small amounts of electrical power and were extremely lightweight. The next question was, how well would these integrated silicon circuits stand up in the harsh radiation environment of space?

This question has been the topic of many papers, conferences and publications in the last 25 years. This thesis can be added to that large collection of data. The experimental data obtained will enable satellite designers in the future to determine how capacitors and possibly other CMOS VLSI components behave while they are being subjected to largedoses of radiation.

B. THESIS ORGANIZATION

This thesis is organized to provide the reader with a basic background knowledge of space radiation environments (Chapter II), ways radiation affects matter, specifically silicon (Chapter III) and how MOS capacitors are fabricated (Chapter IV). Chapter V is devoted to the experimental set up including; a description of the VLSI chip used, a description of the circuit used in testing the capacitors and the setup and use of the NPS

Linear Accelerator (LINAC). Chapter VI presents the results obtained and Chapter VII discusses the conclusions and recommendations. There are also 2 appendices, Appendix A The Specialty Chip, is a description of a specialized chip designed for this type of testing and Appendix B Experimental Data, lists all the tabulated results.

II. RADIATION ENVIRONMENT IN LOW EARTH ORBITS

A. RADIATION TYPES AND INTERACTIONS

There are several types of radiation that come into play in the space environment. These types of radiation can be divided into 2 classes. The first class is particles. This class would include heavy ions (Lithium and up), alpha particles (helium nuclei), beta particles (high speed electrons), neutrons, protons, neutrinos, antineutrinos and positrons. The second class of radiation is photons or electromagnetic wave packets. These wave packets or quanta contain energy and momentum but are essentially massless. The most common are gamma rays and X-rays. In space, all forms of radiation exist and probably even more which have not been discovered. The research in this thesis involves the use of electrons from a linear accelerator (LINAC). These LINAC electrons closely resemble beta particles. A brief discussion of the most common radiation forms follows.

1. Particles

There are three types of particles; positively charged, negatively charged and those with no charge or neutral charge. The neutrally charged particles are neutrons, neutrinos and antineutrinos. The positively charged particles are, the alpha particle, the proton and the positron. The negatively charged particle is the beta particle (a high speed free electron). The particles of most interest are the heavy ion (including the alpha particle), the beta particle, the proton and the neutron. These particles are the most common in space.

a. Positively Charged Particles

Alpha particles, protons and positrons are the positively charged particles discussed here. Protons, (ionized hydrogen) are trapped in the outer Van Allen belt. Positrons are merely positively charged electrons. These are formed during "pair production" a form of photon-atom interaction. Another particle of concern is the alpha particle. This particle is actually the nucleus of a Helium atom. It contains 2 protons and 2 neutrons giving it an atomic mass of 4. The alpha particle has no electrons thus it has a positive net atomic charge of +2 due to the presence of the 2 protons. The alpha particle is formed as a result of radioactive decay from specific atomic isotopes. It can also be formed during fission or fusion. The sun and other stars operate on the fusion principle thus providing a plentiful source of alpha particles in space.

Additionally there are heavier ions then the alpha particle. These ions are heavier atoms which have their electrons stripped away. These are not as plentiful in the space environment.

b. Negatively Charged Particles

Another type of charged particle is the negatively charged high speed free electron or beta particle. This particle has a net negative atomic charge of 1 and the mass of a normal electron at rest (9.1091E-28 grams). These particles are formed from the radioactive decay of specific isotopes and from nuclear fission or fusion. Beta particles like alpha particles and protons are very plentiful in space.

c. Neutral Particles

The last type of particles are those with no charge, the neutron, the neutrino and the antineutrino. The neutrino is a particle with a very small rest mass. It was originally postulated to exist to account for the continuous energy distribution observed during the beta decay process. The antineutrino has been theorized to exist due to unexplainable non-conservation of energy during a beta decay. Although the study of neutrinos and antineutrinos has escalated in the past few years they will not be discussed here. The neutron is the major particle of interest when studying nuclear fission. It has the same rest mass as a proton but has no atomic charge. Neutrons are produced from radioactive decay and from fission and fusion. In fact the basic operation of all nuclear fission reactors is based upon the production of neutrons from fissioning atoms.

The Largest concentration of neutrons in space occurs about 50,000 feet above the earth. In this vicinity cosmic rays interact with atmospheric oxygen and nitrogen to create these neutrons.

2. Photons

Photons are non particle forms of radiation. They are quantized packets of electromagnetic radiation. They have no rest mass but they exhibit momentum. These quantized packets interact with matter in three different ways, 1) photoelectric effect, 2) Compton scattering, and 3) pair production. Figure 2.1 illustrates the three types of interactions as well as the relative energy levels at which each is most prevalent.

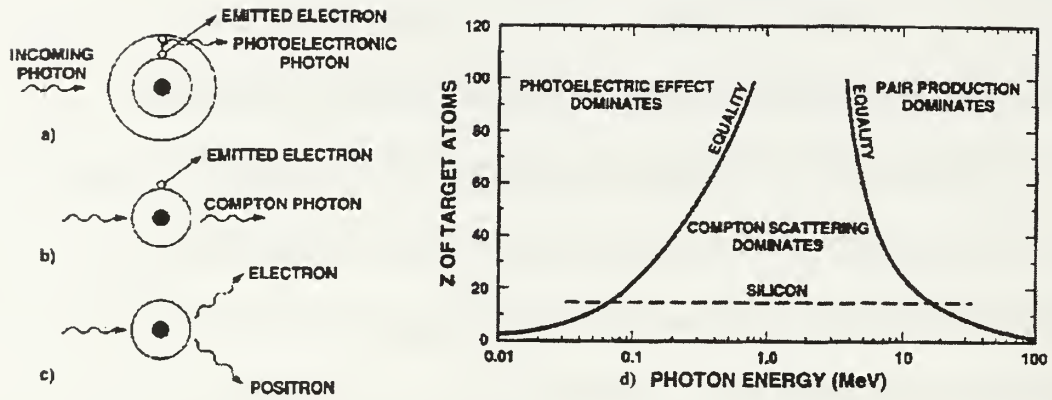


Figure 2.1 An illustration of photon interactions a) Photoelectric Effect, b) Compton Scattering, c) Pair Production, also a graph of atomic mass versus energy showing the most probable energies associated with each. After Ref. (Schwank, 1994, p. II-15 & 16)

a. Photoelectric effect

In this interaction the photon packet is absorbed by an atom. The energy from the photon is transferred to one of the outer valence electrons of the atom. The energy transfer causes the electron to jump to a higher energy level or state. With the electron in the higher state the atom is unstable. The excited electron drops back into the lower energy level or state releasing the stored energy it gained when the incident photon was absorbed. This released energy goes out in the form of another photon. Sometimes the electron can actually be emitted which is called Compton scattering described below.

Photoelectric effect requires the least energetic photons of the three types of photon interactions. Photons of less then 70 keV can cause the photoelectric effect.

b. Compton Scattering

In this photon-atom interaction the photon is once again absorbed by the incident atom. The increase in energy in the atom causes one of the outer electrons to

escape from its normal energy state and fly off into space as a free electron (beta particle). Any left over energy is then emitted in the form of a Compton photon. The Compton photon has less energy then the original incident photon.

Compton scattering is the predominant photon interaction involving photons with energies between 70 keV and 20 MeV.

c. Pair Production

In pair production once again the electron is absorbed by an atom. After absorption the incident atom emits two particles, an electron and a positron. This interaction takes place only if incident photon energies are above 1.02 MeV. Photons with enough energy to cause pair production are normally not found in space.

B. BRIEF HISTORICAL OVERVIEW OF SPACE RADIATION

With a basic background in types of radiation, a discussion of the most common types of radiation in space is in order. Until the 1950's science had very little information regarding the radiation environment in space. The first real attempt to map the space radiation environment came in January of 1958 when Explorer I was launched carrying a Geiger counter. The satellite had no onboard data storage capability so it provided limited information in the form of counter readings relayed to the ground station when it was within transmission range. Even with the lack of data collection ability an anomaly was discovered to exist at high altitudes over South America. Later when Explorer III was launched with onboard recording devices an area of extremely high particle flux was discovered over South America and named the South American Anomaly (SAA). The discovery of the SAA prompted more spacecraft with more sophisticated recording

equipment. Explorer IV and the Pioneer series, specifically Pioneer III, were very instrumental in the collection of data. Using the data collected from these missions Professor Van Allen from Iowa University developed a rough map of the radiation belts above the earth (see Figure 2.2) This map illustrated the concept of inner and outer radiation zones much the way we understand them today. (Tabbert, 1993, p. 2.1-2)

Once Van Allen created his first radiation belt mapping, more sophisticated methods were employed to map these anomalies.

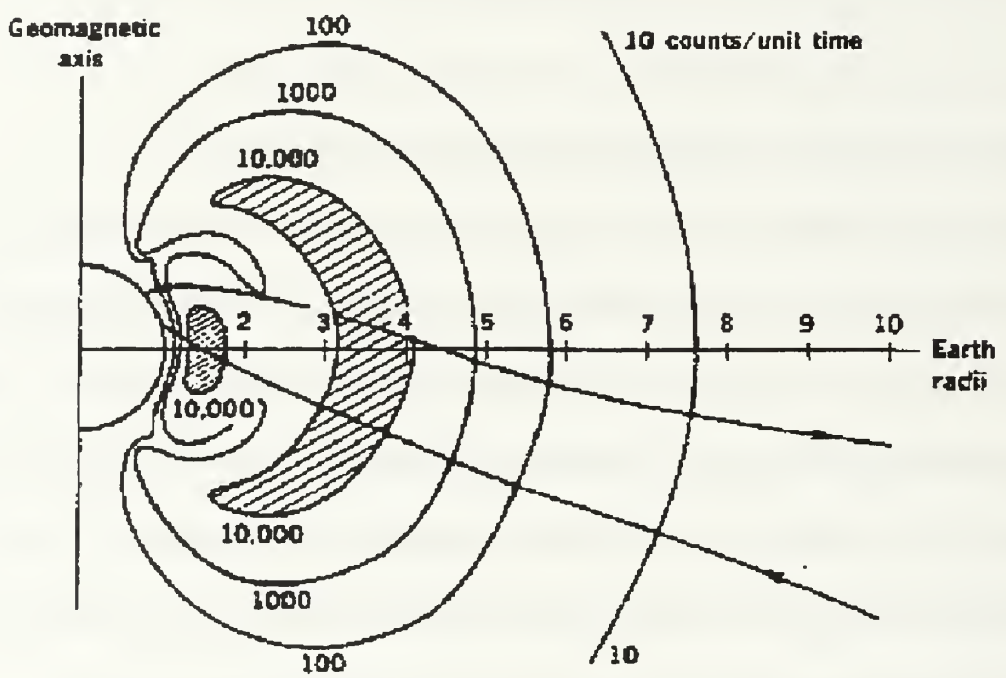


Figure 2.2 Van Allen's map of the radiation belts. From Ref. (Corliss, 1993, p.39)

C. THE NATURAL SPACE ENVIRONMENT

There are 3 classifications or types of radiation in the natural space environment. One is characterized by particles trapped in the Earth's magnetic field. The other two types are forms of cosmic rays.

1. Cosmic Rays

Cosmic rays were first discovered in 1911. There are two sources of cosmic rays, galactic cosmic rays (originating outside our solar system) and solar cosmic rays (originating from the sun). Solar cosmic rays may also be called solar plasma. Galactic cosmic rays make up the majority of cosmic rays. Solar cosmic rays, which exhibit a flux change from day to night, are usually only a small portion.

a Galactic Cosmic Rays

The vast majority of cosmic rays come from outside the solar system. These rays are called galactic cosmic rays. The likely sources for galactic rays are the stars in the Milky Way and in other galaxies. Galactic cosmic rays are composed of mostly protons (89%) and alpha particles or helium nuclei (9%). The other particles found in cosmic rays include beta particles (electrons), gamma rays and heavy ions (about 2%). The heavier ions posses very high energies on the order of 0.1 to 1 GeV. These heavy energetic ions can cause significant damage in electronic circuitry due to their high energies. The interactions between galactic cosmic ray protons and the earth's atmosphere create electrons, neutrons and gamma rays. The interactions of these other types of radiation sources with electronic components can causes damage. (Ricketts, 1972, p. 461)

b. Solar Cosmic Rays

Solar flares are generally responsible for solar cosmic rays or solar plasmas. They are linked to the solar activity cycle. These solar plasmas caused by solar flares are electrically neutral due to the equal number of positive and negatively charged particles. This solar plasma is actually an extension of the suns corona. The contents of the solar plasmas are roughly the same as galactic cosmic rays and therefore interact the same with the earth's atmosphere. After a solar flare, particles begin to arrive at the earth's magnetosphere in minutes. The resulting radiation increase can last up to 2 weeks. This increase in radiation, caused by solar plasmas, can increase radiation effects up to 10,000 times that of galactic cosmic rays. (Schwank, 1994, p. II-8)

2. Trapped Particles

The Earth is encased in a non-uniform enclosure called the magnetosphere, see Figure 2.3. This magnetosphere consists of magnetic field lines which trap charged particles. The shape of the magnetosphere can be seen in Figure 2.3. It is hemispherical on the day side, with a radius of about 10 times the of the radius of the earth (Earth's radius is 6378 km (3963 miles)). On the night side, it is an extremely long cylinder, hundreds of earth radii in length. It has an approximate diameter of 40 times that of the earth. The shape of the magnetosphere is caused by the solar wind (solar plasma).

The area of interest for particle trapping is, where the majority of earth bound satellites reside. This relatively small region is called the plasmasphere. Typically, the plasmasphere is made up of relatively lower energy protons and electrons but some heavier ions may also be trapped here. The trapped particles move in a spiral direction

around the magnetic field lines. They also bounce back and forth from pole to pole along these same field lines as illustrated in Figure 2.4. The particles also drift around the Earth in an orbital pattern. Electrons move to the east and protons move to the west. These moving ions along with other trapped particles are what constitute the Van Allen radiation belts. Table 2.1 shows the characteristic time scales for a typical 1 MeV particle with an altitude of 2000 km. (Abrahamson, 1995, pp. 7-8)

The effect of large highly energetic particles contribute to the overall radiation flux in all orbits. Protons and electrons, some of which are trapped and some of which come from cosmic rays, also contribute to this overall flux.

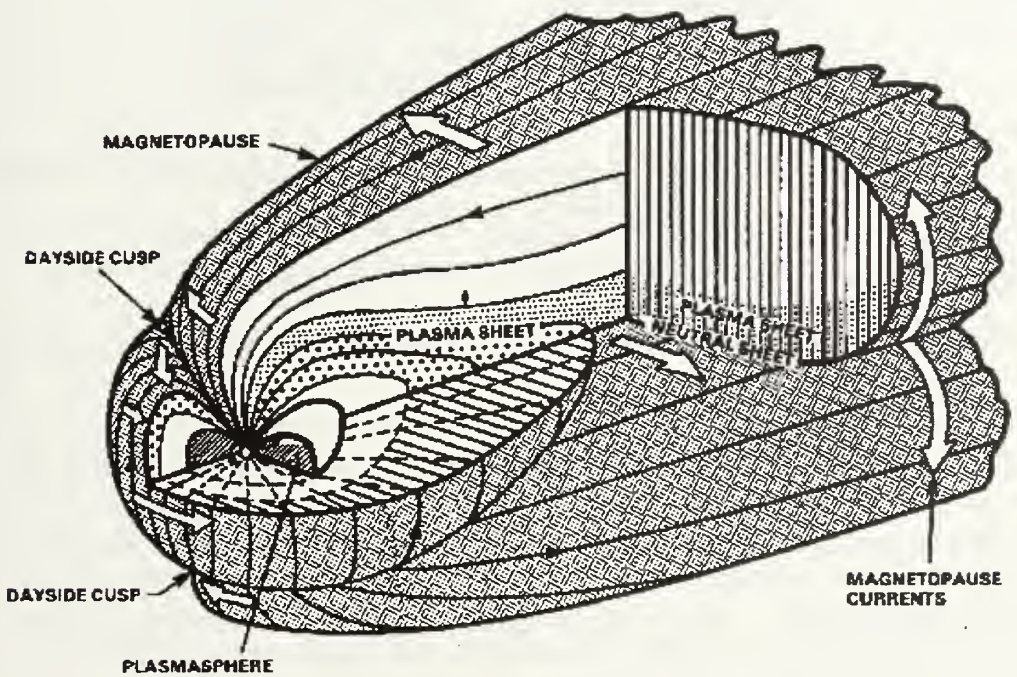


Figure 2. 3 The Magnetosphere. From Ref. (Stassinopoulos, 1988, p. 1424)

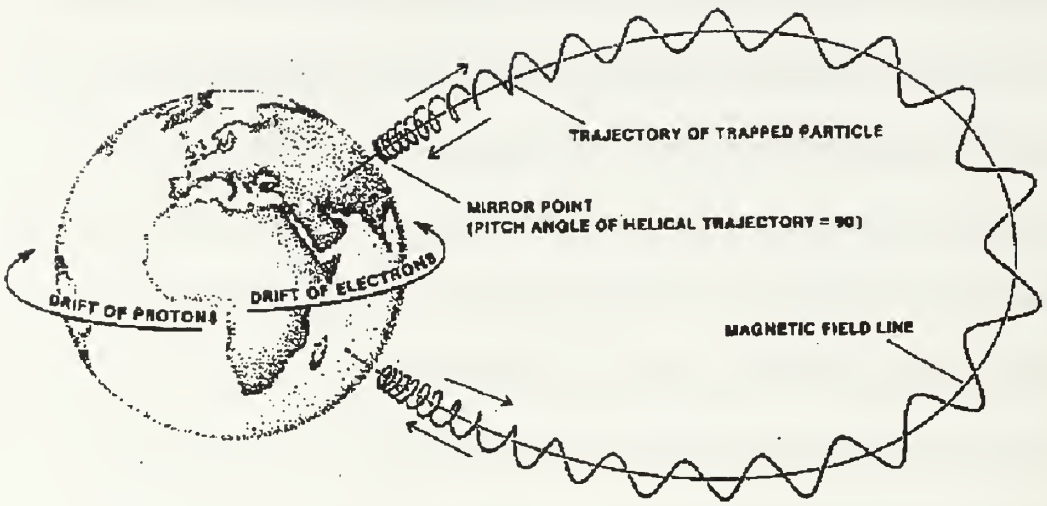


Figure 2.4 Trapped particle motion. From Ref. (Stassinopoulos, 1988, p. 1425)

	Electrons	Protons
Gyration Period	7.0 x 10E-6 seconds	4.0 x 10E-3 seconds
Bounce Period	0.1 seconds	2.2 seconds
Drift Period	53 minutes	32 minutes

Table 2.1 Characteristic particle motion time. From Ref. (Abrahamson, 1995, p. 9)

There are obviously different levels of radiation depending upon where a satellite is located in the magnetosphere. Figure 2.5 illustrates a breakdown of 5 specific regions and the types of particles which predominate in these regions.

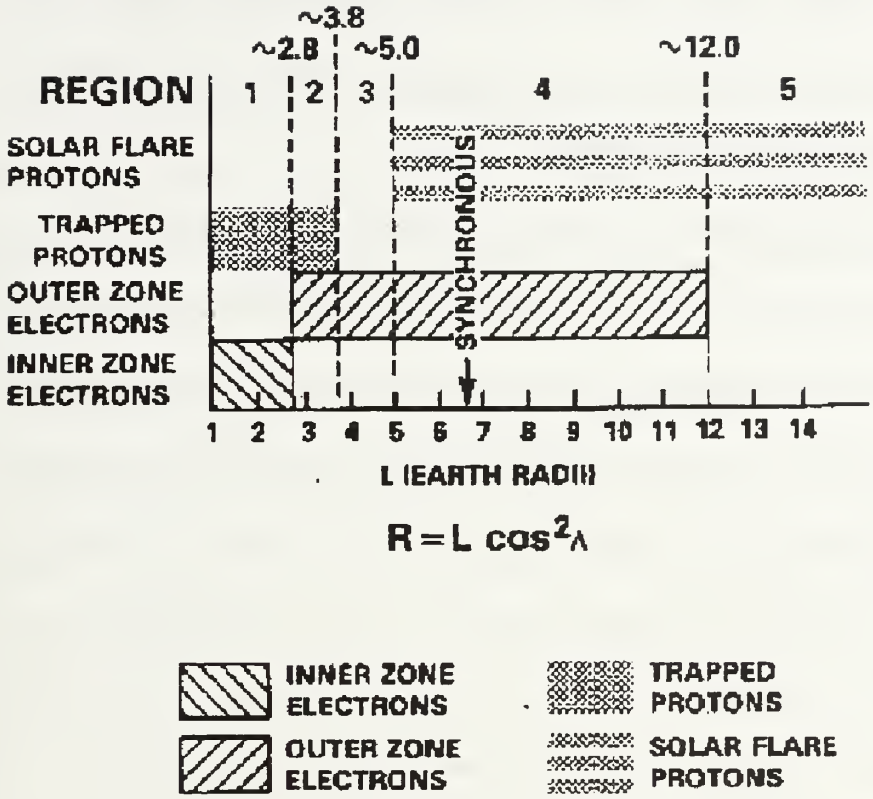


Figure 2.5 The distribution of charged particles in the Magnetosphere. From Ref. (Stassinopoulos, 1988, p.1425)

The two factors which geolocate a satellite are altitude (distance from the earth) and inclination (distance from the pole in degrees). A close examination of Figure 2.1 shows that the shaded areas (representing higher concentrations of trapped particles) are located above the equator and away from the poles. This phenomena provides for the following conclusion applicable to LEO satellites. Low concentrations of radiation exist at low altitudes and high inclinations (high latitudes). While the higher concentrations of particles thus the higher radiation areas are located at small inclinations (lower latitudes) and higer altitudes (Brittain, 1995, p.22). This generalization illustrates how satellites

are influenced by radiation in earth orbits. The majority of the trapped radiation received by satellites in Low Earth Orbits (LEO's) comes from the SAA mentioned previously.

D. LEO RADIATION ENVIRONMENT

Modeling the actual radiation environment for satellites is very difficult. The simplified discussion, given above, does not due justice to the complex reality of space radiation. This thesis will not attempt to determine the exact levels of radiation received by satellites in earth orbit. The purpose of the brief explanation given here is to provide some background information on the different types of radiation in space and how they interact with matter. The overall conclusion is, satellites which pass through the Van Allen belts will receive higher doses of radiation from the trapped particles than satellites that do not pass through these belts. Satellites that have high inclinations and low altitudes tend to avoid the Van Allen belts. These low orbit satellites are also shielded from cosmic rays by the earth's extended atmosphere. Once again the idea of using LEO satellites from a radiation standpoint appears valid.

III. MOS CAPACITOR FUNDAMENTALS

The fundamentals of MOS capacitor design and operation are essential to understanding the testing done in Chapter V. Additionally, the description of radiation damage mechanisms in Chapter IV will be easier to understand given the information presented here.

A. FUNDAMENTAL MOS CAPACITOR OPERATION

MOS capacitors can be biased either positively or negatively. This simply means the top plate of the capacitor may have a negative or positive charge with respect to the bottom plate. (Grebene, 1984, p. 165) The different effects caused by these two types of biasing will be discussed for ideal parallel plate MOS capacitors. A discussion of non-ideal work functions and trapped charges will then be addressed.

1. The Ideal Capacitor

With no voltage applied to an ideal MOS capacitor the work function difference, $q\phi_{ms}$, is ideally equal to zero as seen in Equation 3.1 and in Figure 3.1. The work function difference is simply the difference between the work function of the metal or top layer ($q\phi_m$) and the semiconductor or, bottom layer ($q\phi_s$). There may be several layers in a multi-layer capacitor, this would add the work function effect. However, a single layer example provides an adequate illustration of the work function effects.

$$q\phi_{ms} \equiv q\phi_m - \left(q\chi + \frac{E_g}{2} + q\psi_B\right) = q\phi_m - q\phi_s = 0 \qquad (3.1)$$

where

$q\chi$ = semiconductor electron affinity

$q\psi_B$ = energy difference between the Fermi and intrinsic Fermi levels

With no bias voltage the conduction energy level (EC) and valence energy level (EV) both appear flat. This is termed the Flat Band Voltage. In an MOS capacitor there is no carrier transport through the oxide layer. This means, it has virtually infinite resistance. The only charges that exist are adjacent to the top and bottom plates. Biasing a MOS capacitor creates three possibilities for altering the band gap energies, Accumulation, Depletion and Inversion. (Sze, 1985, p. 187)

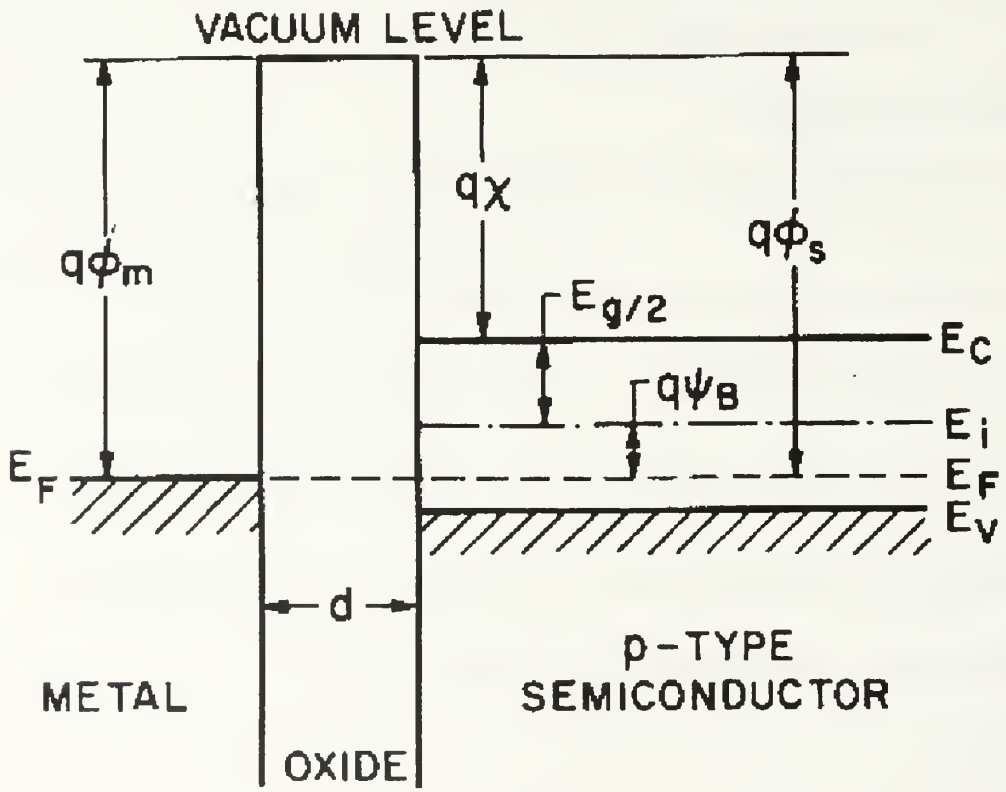


Figure 3.1 The flat band energy diagram illustrating the work functions and the energy levels in a bi-layer MOS capacitor. From Ref. (Sze, 1985, p.187)

a. Accumulation

If a positive voltage is applied to the top plate, an overall negative bias (V < 0) is created. In this case, the mobile holes are attracted to the surface of the semiconductor and the energy bands bend upward as seen in Figure 3.2 (a). Since no charges can flow through the oxide layer, the Fermi level remains constant. This allows for an increase or accumulation of holes at the oxide-semiconductor boundary. A more detailed explanation of how carrier densities at the conduction and valence energy levels are effected by the location of the Fermi energy level can be found in Sze, (1985, p. 22-2).

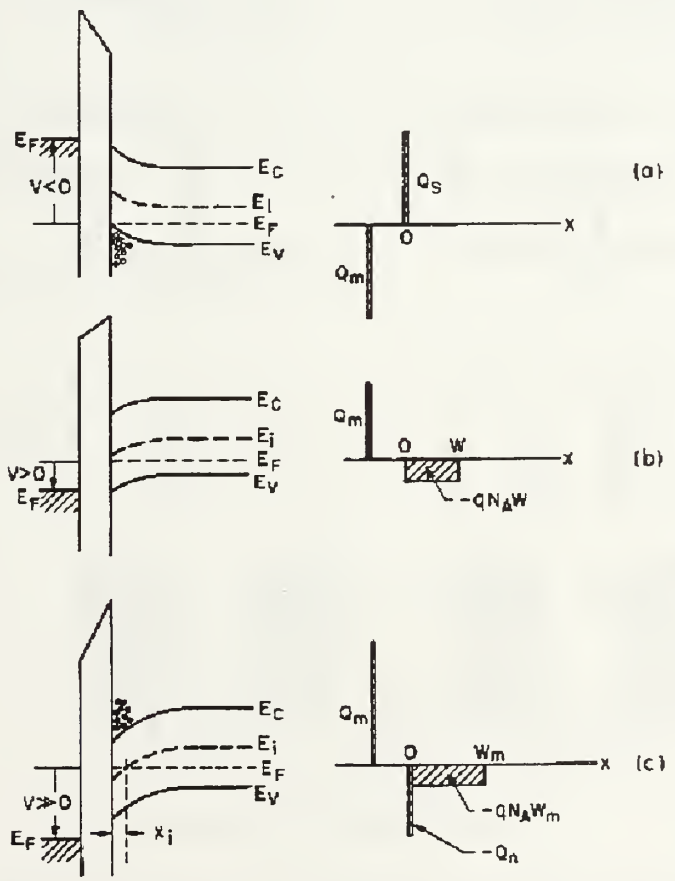


Figure 3.2 Ideal MOS capacitor energy level diagrams and charge distributions (a) Accumulation, (b) Depletion, (c) Inversion. From Ref. (Sze, 1985, p. 188)

This relationship is illustrated in Figure 3.3. There is an excellent explanation of the relationships of these energy levels in Abrahamson, (1995, p. 26-30).

b. Depletion

When a small negative voltage is applied to the top plate the capacitor is biased slightly positive (V > 0). This causes the energy levels to be bent down. The majority carriers, in this case holes, are depleted in a region with width, W, as seen in Figure 3.2 (b).

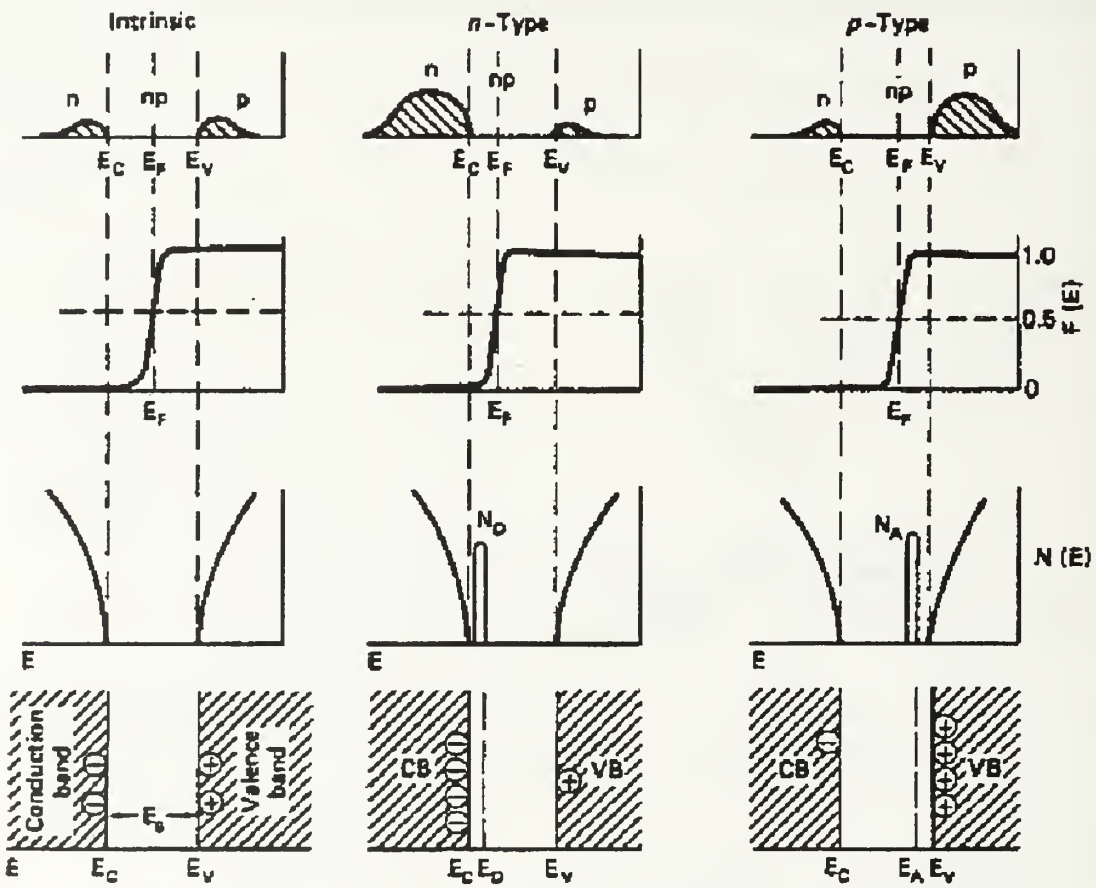


Figure 3.3 A summary view of the intrinsic and extrinsic carrier densities, Fermi levels and energy bands. From Ref. (Messenger, 1992, p.16)

c. Inversion

The third phenomena takes place when the bias voltage is made very positive (V >> 0). In this situation the energy levels continue to bend down as seen in Figure 3.2 (c). In this condition the Fermi level is actually higher then the intrinsic level. The Fermi level to intrinsic level difference becomes positive (p-type to n-type) which leads to an exponential increase in the number of electrons. Electrons in this situation are supposed to be the minority carriers, however, since they outnumber the majority carrier the resulting charged surface is termed inverted. As voltage is further increased the conduction band will approach the Fermi level and electron concentration will increase rapidly. This leads to the formation of a very thin layer of negative charge called the inversion layer. The width of this layer is typically much thinner than the surface depletion layer. Once the inversion layer forms, the depletion layer reaches its maximum thickness W_{max} (see Equation 3.2).

$$W_{\max} = \sqrt{\frac{4\varepsilon_s kT \ln(N_A/n_i)}{q^2 N_A}} \qquad (3.2)$$

Where

k = Boltzmann's constant (8.63 E -5 eV/K)
T = temperature in K
N_A = Acceptor ion concentration
n_i = intrinsic carrier density (1.45E10 carriers/cm^2 for silicon)
q = electron charge (1.602E-19 C)
ε_s = permittivity of silicon (F/cm)

Once a strong inversion layer is formed, any further bending of the energy levels will cause a small increase in the depletion layer width. The charge on the inversion layer will continue to increase. (Blicher, 1981, p.3-16) (Sze, 1985, p. 186-189)

d. Ideal Capacitance Calculation

The ideal MOS capacitance is simply the series connections of the oxide layer capacitance, C_{ox} and the depletion layer capacitance, C_s. A detailed description of the depletion layer of P-N junctions can be found in Sze, (1985, p. 70-80). A more condensed explanation is found in Abrahamson, (1995, p.26-30). The total capacitance to oxide capacitance ratio can be found using Equation 3.3.

$$\frac{C}{C_{ox}} = \frac{1}{\sqrt{1+\left(2\varepsilon_{ox}V_g/qN_A\varepsilon_s t_{ox}^2\right)}} \qquad (3.3)$$

where

V_g = Gate Voltage
ε_s = silicon permittivity
ε_{ox} = oxide permittivity
t_{ox} = oxide thickness

2. Non-Ideal Characteristics

The above explanations were for idealized capacitors. In the real world several factors affect the ideal operation of an MOS capacitor; the work difference function, the presence of trapped charges in the oxide and semiconductor and the effect of these charges on the flat-band voltage. These are just three of the non-ideal situations which may come into play.

a. Work Difference Function

The ideal work function difference is zero as described above. Realistically this is not the case. Normally $q\phi_m$ is smaller then $q\phi_s$, this causes the difference to be negative. The net result is that some electrons leave the metal and migrate to the p-type silicon via an external path around the oxide layer. The metal plate gains a slight positive charge and repels holes causing uncompensated negative acceptors to appear near the semiconductor surface. This charge separation creates a potential difference in the oxide and the depletion regions equal in magnitude but opposite in sign to the work function. (Sze, 1985, p. 195-197) (Blicher, 1981, p. 3-6)

b. Charge Trapping, Fixed Oxide and Mobile Ionic Charges

There are several other effects which cause non ideal situations to exist in an MOS capacitor. These include, interface traps, oxide traps, border traps, fixed oxide charges and mobile ionic charges.

The first of these non-ideal situations is the interface trap (Q_{it}). These traps are caused by irregularities in the silicon and silicon dioxide lattices. These irregularities depend largely on the chemical structure at the Si-SiO_2 interface during fabrication. These traps have energy levels which lie in the forbidden Si energy gap. The concentration of these interface traps is highly dependent on the crystalline structure of the silicon. The number of interface traps can be reduced by annealing the silicon and silicon dioxide at low temperatures (450° C). These types of traps can also be created by ionizing radiation as discussed in Chapter IV. (Sze, 1985, p.197) (Blicher, 1981, p.6-19)

The next non-ideal charge type is the fixed oxide charge (Q_f). These fixed charges are located within 30 Angstroms of the Si-SiO_2 interface. This charge is normally positive and is also highly dependent on the crystalline structure of the Si and the SiO_2. It also depends on the oxidation and annealing conditions during fabrication. A possible explanation as to the cause is due to uncompleted Si bonds remaining near the surface following the growth of the SiO_2 layer. (Sze, 1985, p. 198)

The third charge type consists of mobile ion charges (Q_m). These ions are non-intentional impurities in the SiO_2 layer. These ions are highly mobile especially at higher temperatures. They are predominantly positive and hence migrate to the Si-SiO_2 interface under an applied positive gate voltage. This elevated positive charge at the interface causes a large change in the expected capacitance. This change is not permanent because the ions will shift the other direction if the biasing voltage is reversed. The ease at which these ionic charges move within the oxide layer gives rise to device instability in the capacitor. The only way to reduce these charges is to remove as many causes for impurities as possible. This is done by furnace wall cleaning, gas purification during the oxidation process and ensuring the Si crystal surface is maintained as pure as possible. (Blicher, 1981, p.21)

The final type of trapped charges is the oxide trapped charge (Q_{ot}). These are actually trapped inside the lattice structure of the SiO_2. They are normally created by

exposure to radiation fluxes (see Chapter IV). Figure 3.4 depicts relative locations of the different trapped charges.

c. Flat Band Voltage

All of the non-ideal charges found in the SiO_2 layer change the flat band voltage. This change is reflected in Equation 3.4.

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_o} \qquad (3.4)$$

The effects of the non-ideal situations can be seen in the shifted C-V curve of Figure 3.5. Curve (a) is the ideal capacitor. Curve (b) depicts a capacitor with a non-ideal work function and oxide charges. These tend to merely shift the curve. Curve (c) also includes large amounts of interface traps which tend to distort the curve.

B. MOS CAPACITOR STRUCTURE AND DESIGN

The most fundamental design for MOS capacitors consists of two conducting plates electrically isolated by a dielectric normally SiO_2. This simple design will be briefly covered to provide a basic overview of the process involved in VLSI fabrication techniques.

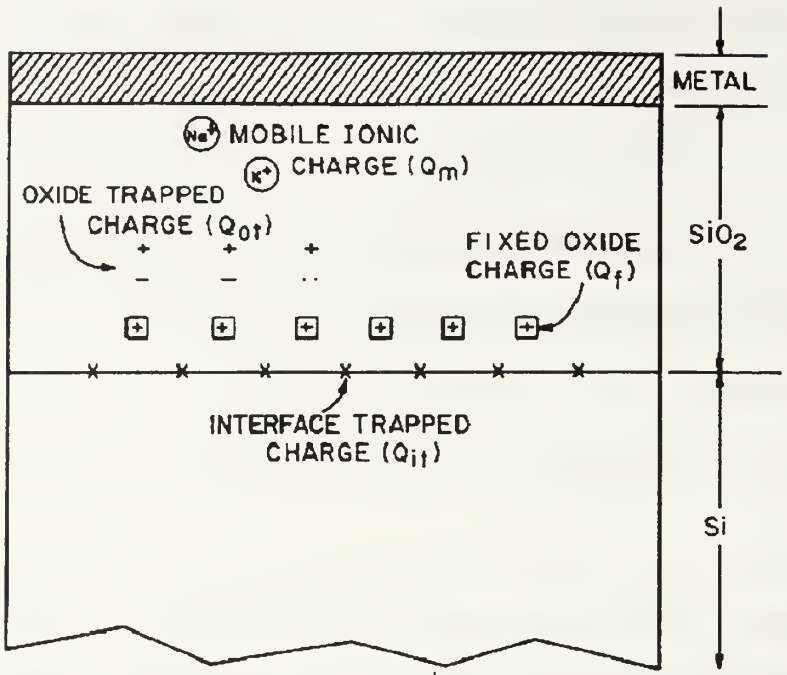


Figure 3.4 Non-ideal charges and traps. From Ref. (Sze, 1985, p. 197)

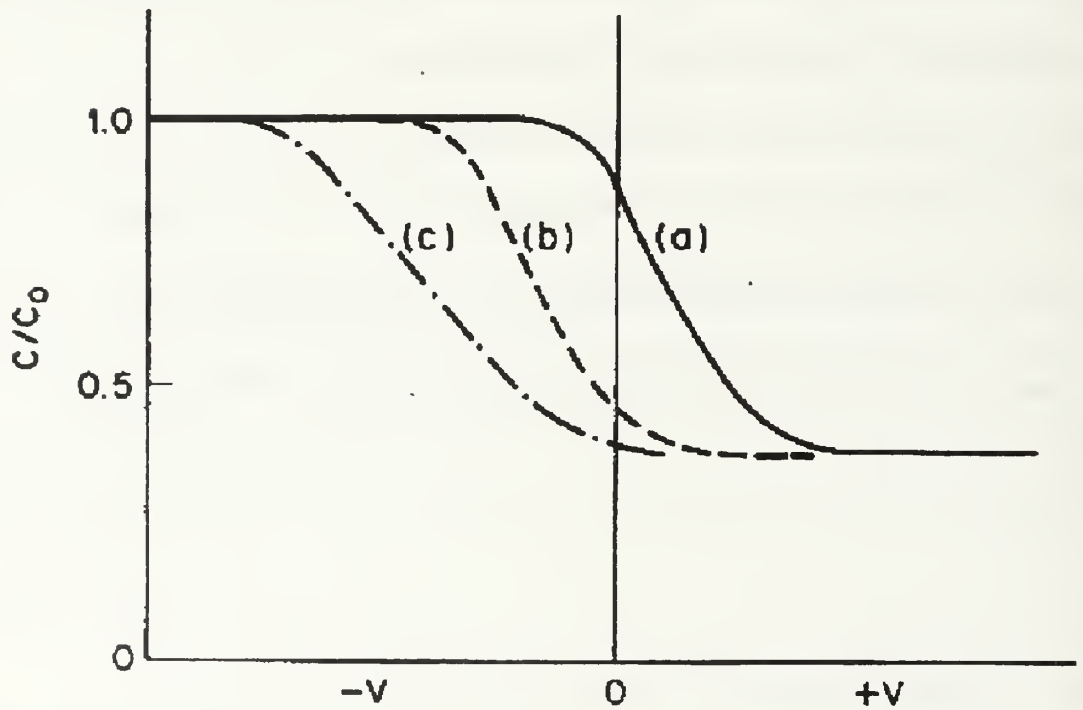


Figure 3.5 The normal C-V curve of a capacitor (a), the curve shifted by a non-ideal work function and oxide traps (b) the curve shifted by interface traps (c). From Ref. (Sze, 1985, p.200)

1. Bottom Plate Formation

Figure 3.6 illustrates the formation of the bottom plate of an MOS capacitor using an n-well process. The n+ diffusion layer of silicon is placed on an n-well inside a p-substrate.

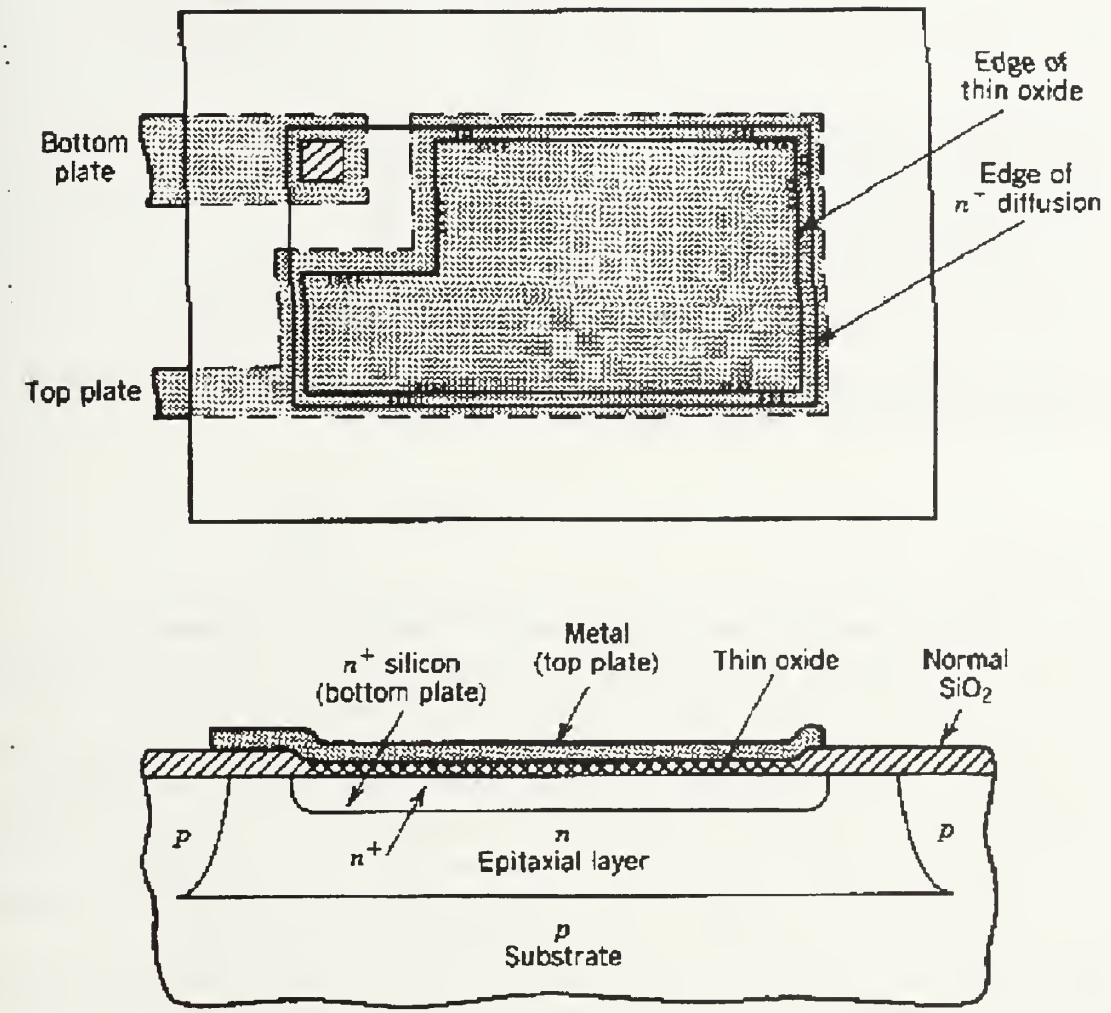


Figure 3.6 The Layout and cross section view of a typical MOS capacitor. From Ref. (Grebene, 1984, p.164)

a. Sheet Resistance

All VLSI components have some sheet resistance associated with them. The plates on an MOS capacitor are no different. The actual resistance of the material on a VLSI chip is given by equation 3.5.

$$R = \frac{\rho L}{WT} \tag{3.5}$$

where

ρ = material resistivity (W/cm)
L = material length (cm)
W = material width (cm)
T = material thickness (cm)

Integrated circuit manufactures prefer to use a similar parameter called the sheet resistance (R_s) defined in equation 3.6.

$$R_s = \frac{\rho}{T} \tag{3.6}$$

The sheet resistance has units of ohms per square unit. To find the total resistance of a given size material, simply multiply the sheet resistance by the length to width ratio. Ideally, the resistance of the capacitor top and bottom plate material is zero. Since this is not physically possible, sheet resistances of a few ohms are typical. There are other device parasitics which can cause capacitors to not perform as ideal. The stray capacitance of the substrate and epitaxial layer p-n junction may cause non-ideal situations. A simplified circuit which depicts an MOS capacitor equivalent circuit is illustrated in Figure 3.7. It is common during the manufacturing process, to minimize the parasitic capacitance by decreasing or completely eliminating the n-type epitaxial layer. (Grebene, 1984, p. 164-166)

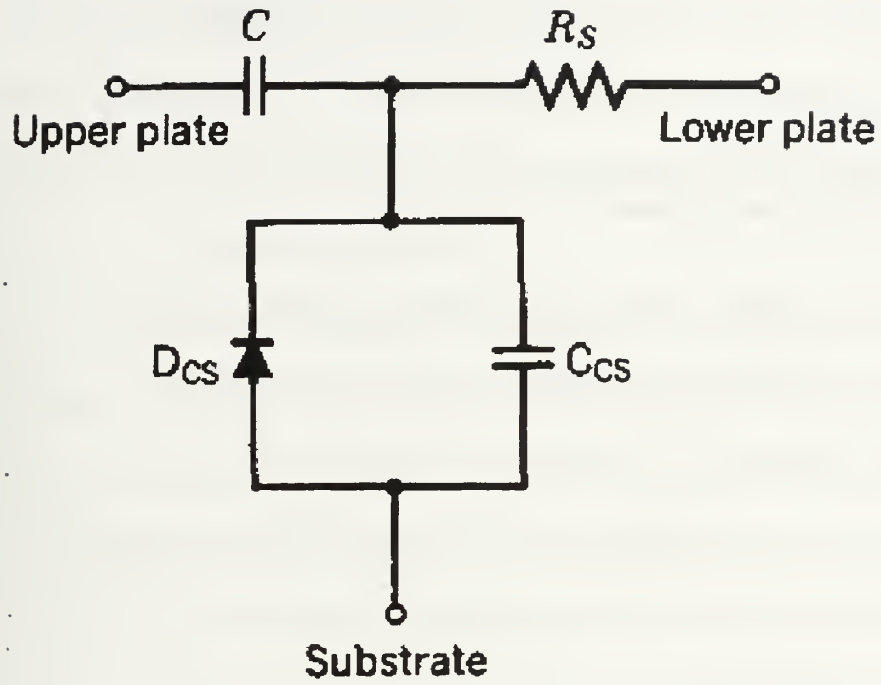


Figure 3.7 A simplified MOS capacitor electrical circuit equivalent diagram. From Ref. (Grebene, 1984, p.165)

b. Emitter Diffusion

One way to construct the bottom plate is using n+ emitter diffusion. Diffusion is the mechanism where different types of particles occupying a given volume tend to spread out and redistribute themselves evenly throughout the volume. Particle diffusion may occur via two mechanisms, substitutional or interstitial. In substitutional diffusion, the impurity atoms replace a silicon atom at a lattice site. In interstitial diffusion, the impurity atoms occupy an interstitial void. Integrated circuit manufacturing primarily uses the first type of diffusion. The particles diffuse according to Fick's Law. The law is illustrated in Equation 3.7.

$$F = -D\frac{\partial N}{\partial x} \tag{3.7}$$

where

N = # particles/unit volume
x = distance measured parallel to flow direction
D = diffusion coefficient (length2/time)

The negative sign indicates the diffusion direction from regions of higher to lower concentration. The diffusion coefficient represents the difficulty of movement an impurity feels, in the lattice structure. It is a property of the impurity and varies exponentially with temperature. In n+ diffusion, a controlled large amount of dopant is introduced into n-type silicon, allowed to diffuse and become the bottom plate of the MOS capacitor. (Grebene, 1984, p. 6-7)

2. Dielectric Layer

A thin oxidized layer of silicon (SiO_2) forms the dielectric region. This oxide layer is generated by heating the silicon wafer to a temperature range of 900-1200° C. An inert carrier gas containing the oxidizing agent, water, is passed over the wafer surface and the following chemical reaction takes place (Equation 3.8).

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \tag{3.8}$$

The oxidation proceeds inward from the surface and slows as the oxidation thickens. For thin layers, a linear growth rate is achievable with respect to time. As the layer thickens the growth rate becomes proportional to the square root of time. The thickness of thermally grown SiO_2 on integrated circuits ranges from 0.05 to 2 μm. The lower limit is

set by electrical breakdown voltages, process control or random defect densities (i.e., pin holes) in the oxide layer. The upper limit is determined by acceptable oxidation times and difficulty of oxide etching during photo-masking. (Grebene, 1984, p. 16)

3. Top Plate Construction

The last step in preparing an MOS capacitor is to deposit an extremely thin layer of conductive material, or metal, on top of the oxide layer. Figure 3.6 illustrates this plate. The top plate completely covers the dielectric and the bottom plate. The metal can be deposited by a variety of methods, two of which are briefly discussed here.

a. Vacuum Evaporation

The capacitor is placed with the conductive element to be evaporated in a bell jar vacuum chamber where pressures range from 10^{-5} to 10^{-6} torr. The metal is heated until vaporization occurs. "Under the high-vacuum conditions used, the mean free path of the vaporized molecules is comparable to the dimensions of the bell jar. Therefore the vaporized material radiates in all directions within the bell jar. " (Grebene, 1984, p. 23) The oxide layer is placed to receive a uniform covering of the vaporized metal. The process is performed at elevated temperatures to ensure good adhesion.

b. Cathode Sputtering

This process also takes place in a low pressure environment. A sputtering apparatus is constructed. A potential of approximately 5000 V is applied between a cathode, coated with the conductive element (metal), and an anode, the oxide layer. There is also an inert gas present in the chamber. The most commonly used gas is argon. Positively ionized argon atoms generated by the anode accelerate toward the negatively

charged cathode. When they impact the cathode they knock off (sputter) metal atoms. Some of these atoms deposit themselves on the oxide layer. Cathode sputtering is much slower than vacuum evaporation.

4. Multiple Layer Capacitors

The above explanation covers the basics of VLSI integrated circuit fabrication techniques, specifically, concentrating on capacitor fabrication. The example used a simple two plate capacitor. There are techniques available to construct multiple layers of conducting material separated by SiO_2 dielectric. A more detailed discussion is presented in Appendix A, which describes the actual design of a specialty chip intended for use in this type of radiation testing.

IV. RADIATION DAMAGE MECHANISMS ON VLSI COMPONENTS

Since all satellites must operate in space and since the radiation environment in space is quite harsh, a brief description of how radiation affects VLSI circuitry is in order. "The manner in which radiation interacts with solid material depends on the type, kinetic energy, mass, and charge state of the incoming particle and the mass, atomic number and density of the target material." (Schwank, 1994, p. II-14)

The actual circuits used in this thesis are fabricated from silicon (Si) and silicon dioxide (SiO_2). There are other materials such as gallium arsinide (GaAs) which can be used to fabricate VLSI circuits. These GaAs circuits tend to be much more radiation tolerant to total dose and transient effects. They also cost more than their counterpart Si circuits. The discussion here will deal with radiation effects on silicon and silicon dioxide since those are the applicable elements in this thesis.

There are two broad classes of radiation effects, ionizing radiation effects and displacement effects. Both of these effects can lead to a third form of radiation damage called charge trapping.

A. IONIZATION

Ionization means to create a charged particle from an uncharged one. This is done in many ways. In silicon based integrated circuits it is accomplished by the interaction of charged particles with the atoms in the silicon and silicon dioxide lattice structure.

1. Charged Particle Ionization Effects

Ionization by charged particles in silicon results in the creation of an electron-hole pair. These pairs are caused by the interaction of the charged particle with an electron bound to one of the atoms in the lattice structure. In order for an ionization to take place enough energy must be transferred from the incident particle to elevate the energy of the bound electron above the energy level of the conduction band in the silicon or the silicon dioxide. The average energy needed to create these electron hole pairs is 3.6 eV for silicon and 17 eV for silicon dioxide. If an incident particle transmits enough energy and exceeds these thresholds an electron-hole pair is produced. Since most incident particles have energy levels well above these thresholds, one particle can produce several thousand such pairs. The majority of particles causing this type of interaction are protons and electrons, both are found abundantly in the earth's magnetosphere. (Schwank, 1994, p. II-17) (Nicollian, 1982, p. 550)

2. Photon Ionization Effects

Photons do not cause a significant number of ionizations in the space environment. They do however contribute to the particle ionization effects in the laboratory. The production of charged particles from these photon interactions is discussed in Chapter II. The free electrons produced by photon interaction can produce the same effects as free electrons in space.

B. DISPLACEMENT AND DEFECT CENTERS

Particles and energetic photons interacting with silicon and silicon dioxide structures can produce a second kind of damage called displacement. The results of these displacements lead to a change in the electron state energies of the Si and SiO_2 structures.

1. Displacement Damage

In displacement damage the incident particle impacts the Si atom or SiO_2 molecule with such force that it moves it out of its lattice structure. This movement is termed displacement. The movement of the atom or molecule creates an interstitial site (a site in the lattice structure which should contain an atom but does not) this is also known as a defect. Compared to ionization displacement damage is rare. Especially when the primary particle of interest is an electron (an electron flux is used in this thesis). The more massive protons and neutrons do much more displacement damage then electrons. The damage caused by displacement is usually permanent. (Nicollian, 1982, p.553)

Displacement ionization can take place due to the covalent bonds which are broken in the process of an atom or molecule being displaced. The vacancy electron-hole pair produced due to these broken bonds is called a Frenkel pair. It requires a minimum of 21 eV for an incident particle to produce a Frenkel pair. (Bourgoin, 1983, p.228-239)

Displacements can cause many different types of defects in the Si lattice structure. A simple point defect involving only one site or a high energy particle interacting to cause several defects. The defects are called clusters. In fact one high energy particle can

cause several clusters while its energy is being dissipated in the surrounding material. An illustration of this is found in Figure 4.1.

These radiation caused defects produce certain types of electrical effects in the surrounding silicon. They tend to create energy levels or states in which electrons can resided that do not correspond to the expected energy states for silicon or silicon dioxide. This is termed defect center electrical effects.

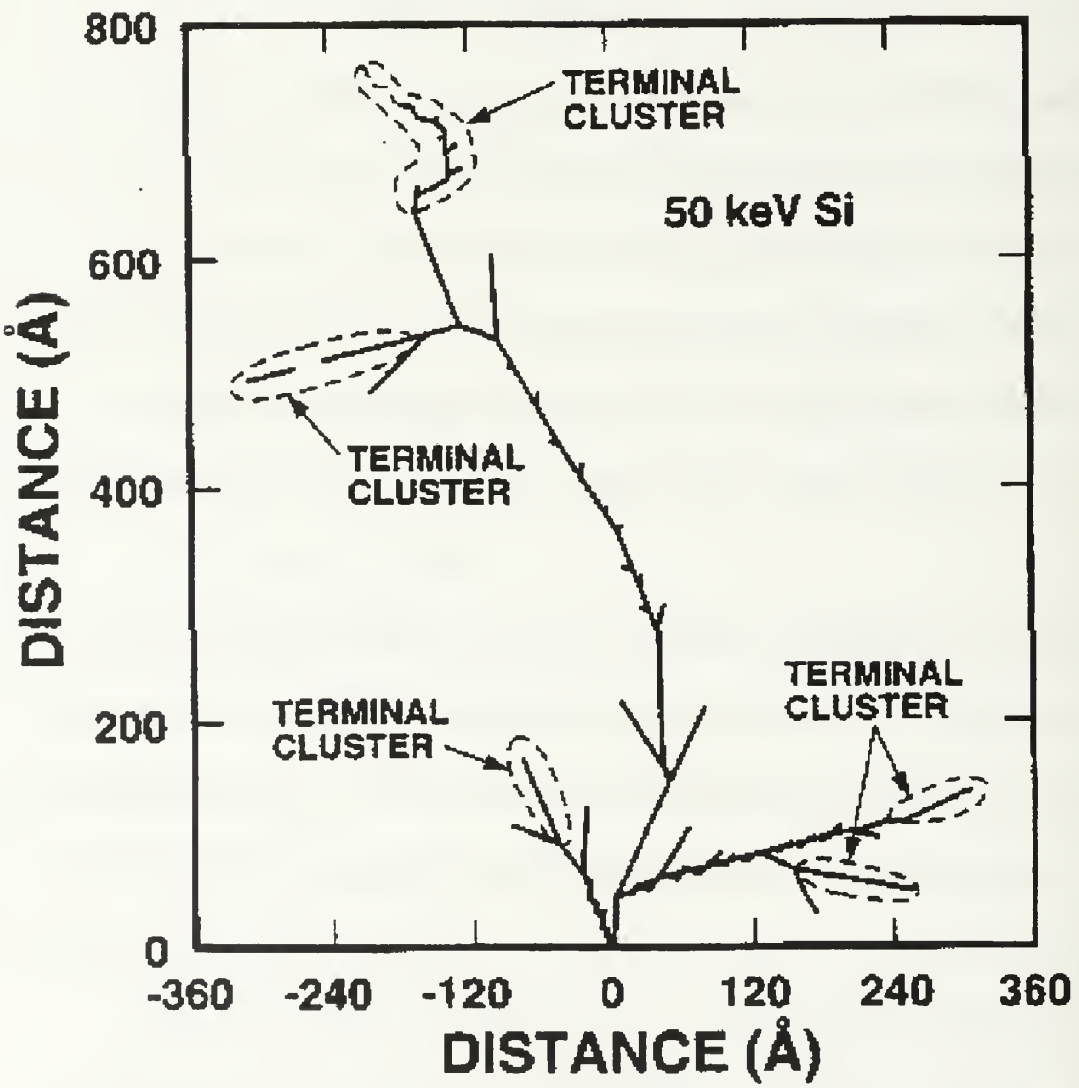


Figure 4.1 Illustration of Cluster formation from a 50 keV recoil atom. After Ref. (Summers, 1992)

2. Electrical Effects from Displacement Caused Defect Centers

The Electrical effects of defect centers come in five different forms, generation, recombination, trapping, compensation and tunneling. They are illustrated in Figure 4.2. The degradation that causes these effects starts with the displacement of the atom from its lattice structure. The loss of the atom from the lattice structure creates new energy levels or states. These new states alter the electrical properties of the device. (This is related to the effects of doping to create p or n type silicon as seen in Chapter III).

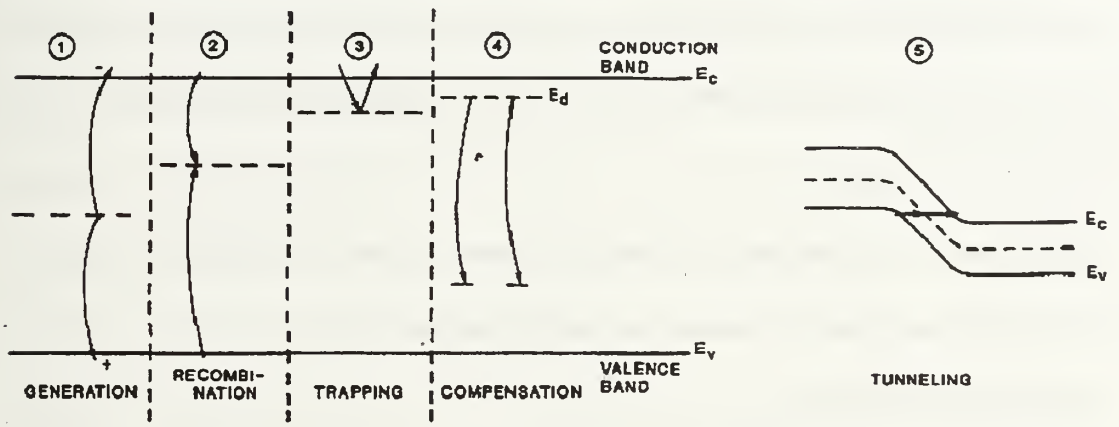


Figure 4.2 Electrical effects caused by defect centers. After Ref. (Srour, 1988, p. 1446)

The first effect, Generation or more appropriately thermal generation, occurs when the defect energy level falls about half way between the valence and conduction bands. As the temperature of the material increases the thermal energy imparted to the electrons in this new energy state is sufficient to cause them to jump or move into the conduction band creating an electron-hole pair.

The next effect is Recombination. Here an electron or hole is trapped by the defect center. This creates an electrical imbalance (a plus or minus charge) this imbalance is corrected by a carrier of the opposite sign also being trapped.

The third effect is Trapping. Here the carriers can be trapped by the defect near their respective normal levels (conduction band for the electron or valence band for the holes). Normally this trapping is temporary. Although if a carrier from the opposite band reaches the site then recombination can occur.

The fourth effect is Compensation. In this mechanism electrons are compensated or removed by deep-lying radiation induced holes in the lattice structure reducing the majority carrier concentration.

The last process is Tunneling. Here the carriers are assisted in crossing the band gap due to modifications caused by radiation damage. (Schwank, 1994, p. II-20)

C. TRAPPED CHARGES

The major cause of radiation damage to silicon and silicon dioxide is charge trapping. Charge trapping is caused by both displacement defects and ionization. In electron radiation fields, like the NPS LINAC, the major cause of radiation damage is ionization. There are three types of commonly considered traps; oxide, interface and border.

1. Oxide Traps

The capacitor must be biased in the positive direction. Without the biasing, very few if any charges will become trapped. While for a very high biasing voltage, the probability of recombination becomes extremely low. The basic mechanism takes place

after some type of ionization. The freed electrons migrate quickly toward the positively charged gate while the holes slowly hop through localized states in the dioxide toward the Si-SiO_2 interface. In oxide trapping they never quite reach the interface and instead build up in the layer near this interface. As they build up they form a positive oxide-trap space charge (See Figure 4.3). (Srour, 1988, p. 1451)

2. Interface Traps

Interface traps lie on the interface between the Si-SiO2 boarder hence the name. These traps are also created under a positive bias. There are two rates at which these traps are produced. The minority of interface traps form in the first few milliseconds of irradiation. The majority of the traps are formed over time. In the space environment with its low level radiation doses, compared to laboratory models, this can happen over several thousands of seconds. The main difference between the interface trap and the oxide trap is their relative charge. Most oxide traps are positively charged (see border traps below). Interface traps, however, can be either positively or negatively charged. The actual charge they exhibit depends on the trap energy level or state (E_t) and its relation to the Fermi level (E_f) of the Silicon. If $E_f < E_t$, the trap will donate an electron to the silicon and become positively charged. If $E_f > E_t$, the trap will accept an electron and become negatively charged. If the two levels are approximately equal, then the trap will have a neutral charge. Another aspect of interface traps is, they do not anneal at room temperature. They are the most important mechanism for low dose rate applications specifically space (see Figure 4.3).

3. Border Traps

Originally it was thought that only interface traps could communicate, change charge based on its trap energy level (E_t), with the silicon layer. This, however, is not the case. Some oxide traps, if close enough to the interface and with the proper trap energy level, may also communicate with the silicon layer. These types of traps have

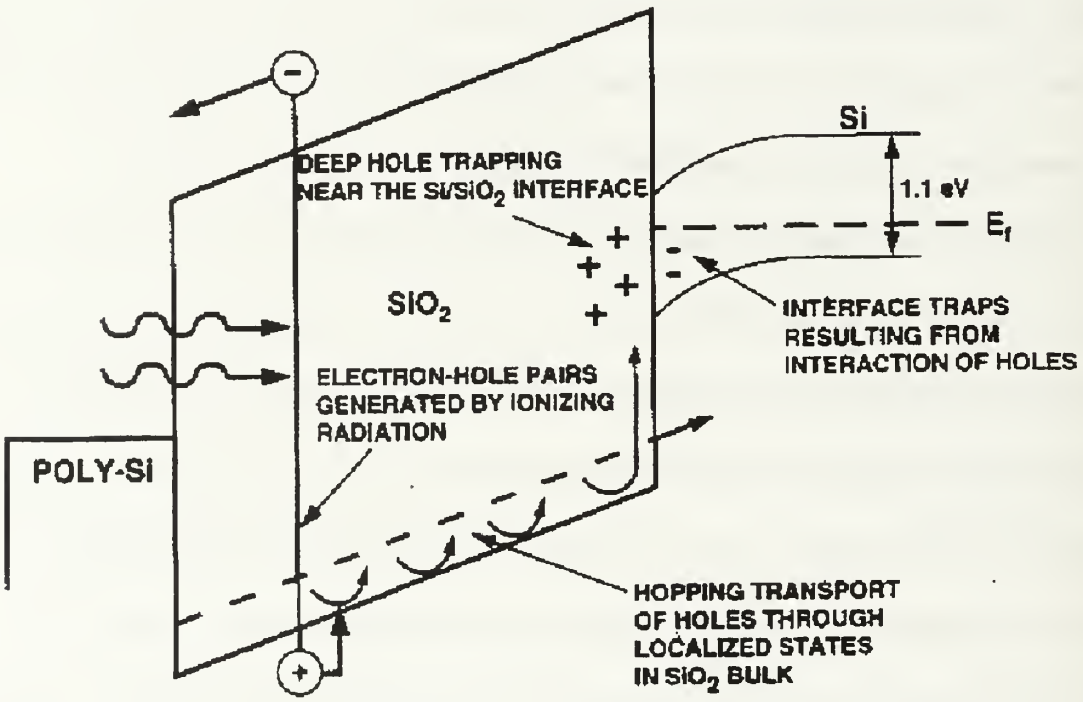


Figure 4.3 The Oxide and the Interface Trap process. After Ref. (Srour, 1988, 1451)

been termed "border traps". Figure 4.4 illustrates the locations of the different traps discussed here. (Fleetwood, 1993, p.5058-5061)

D. SUMMARY

The effects discussed in this chapter are being studied on a macroscopic level in the experimental section of this thesis. The oxide and interface traps cause adverse effects on MOS capacitors as well as transistors. These effects are different under a

radiation flux as compared to after the flux is removed. As mentioned above, with time the radiation induced ionizations can go through a recombination or annealing process and return to a more naturally functioning state. This is the reason for the in-situ testing of the components.

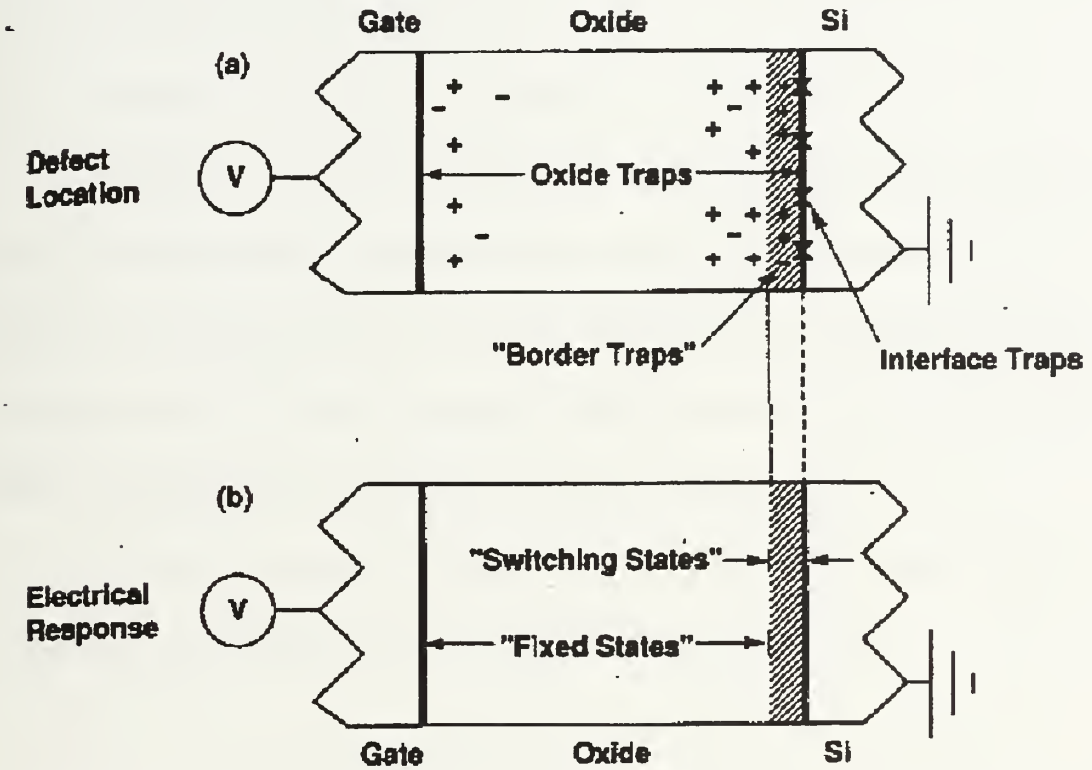


Figure 4.4 (a) the physical location of defects, (b) the electrical response of the defects. From Ref. (Fleetwood, 1993, p. 5059)

V. EXPERIMENTAL SETUP

This chapter explains in detail the setup of the experiment. It includes, a section on the VLSI chip with its capacitors of interest, a section on the circuitry used to test the capacitance during irradiation and finally a section on the setup, calibration and operation of the NPS Linear Accelerator (LINAC).

A. DESCRIPTION OF THE VLSI CHIP

The original VLSI chip designed specifically for this thesis was not available for use. This chip has individual discrete capacitors which can be accessed via external pins. However, there was a problem with the design software and its compatibility with the fabrication facility. As a result, the design was not submitted in time to be used for this thesis. The design of this original chip is covered in Appendix A.

The actual chip used was designed by a former NPS student, Raphael Anestis (Anestis, 1994). A brief discussion of his chip design is included here.

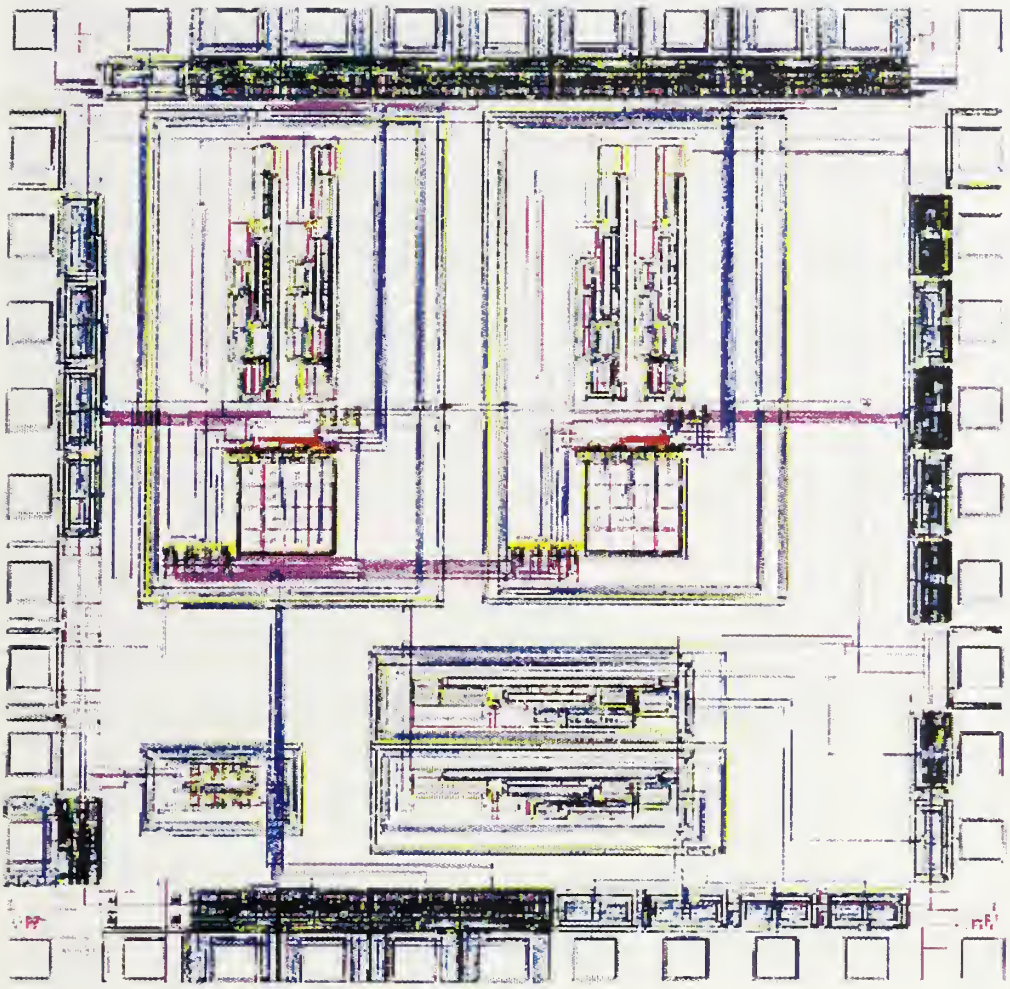


Figure 5.1 The complete microchip layout created using magic. From Ref. (Anestis, 1994, p. 146)

1. Chip Design and Fabrication

The chip produced by Anestis was designed to use switched capacitor networks in conjunction with composite operational amplifiers (COA's). The linking of these two technologies allows circuits to be built as VLSI components. Several masters theses at NPS exist in this area (Bingham, 1993) (Silvernagel, 1993) (Anestis, 1994). The chip was manufactured via the MOSIS fabrication process using orbital 2 micron low noise analog techniques. The detailed parameters of this process are in the thesis by Anestis (Anestis, 1994, p. 141-145). The actual layout of the chip was done using the VLSI design tool "Magic". The actual layout of the chip can be found in Figure 5.1. A floor plan of the chip is also shown in Figure 5.2.

2. The On Chip Capacitors

The part of the chip utilized in this thesis research is the capacitor network. These can best be seen in Figure 5.3. This figure shows the location of the test points relative to the VLSI capacitors on the chip. The switches labeled "odd" and "even" on the diagram represent the even and odd phases of the biphase clock used in the switched capacitor networks. The test points of interest are seen in Figure 5.2 and are labeled V21 and V22. In Figure 5.3, "α*Cr" represents the capacitor network which allows for the programming of the composite op-amp, "Cr" is the one capacitor necessary to allow the switched capacitor function to work and "Cn" is the compensating feedback capacitor necessary to provide stability to the op-amp. The value of Cn is approximately 6 picoFarads and the value of Cr is approximately 1 picoFarad by design.

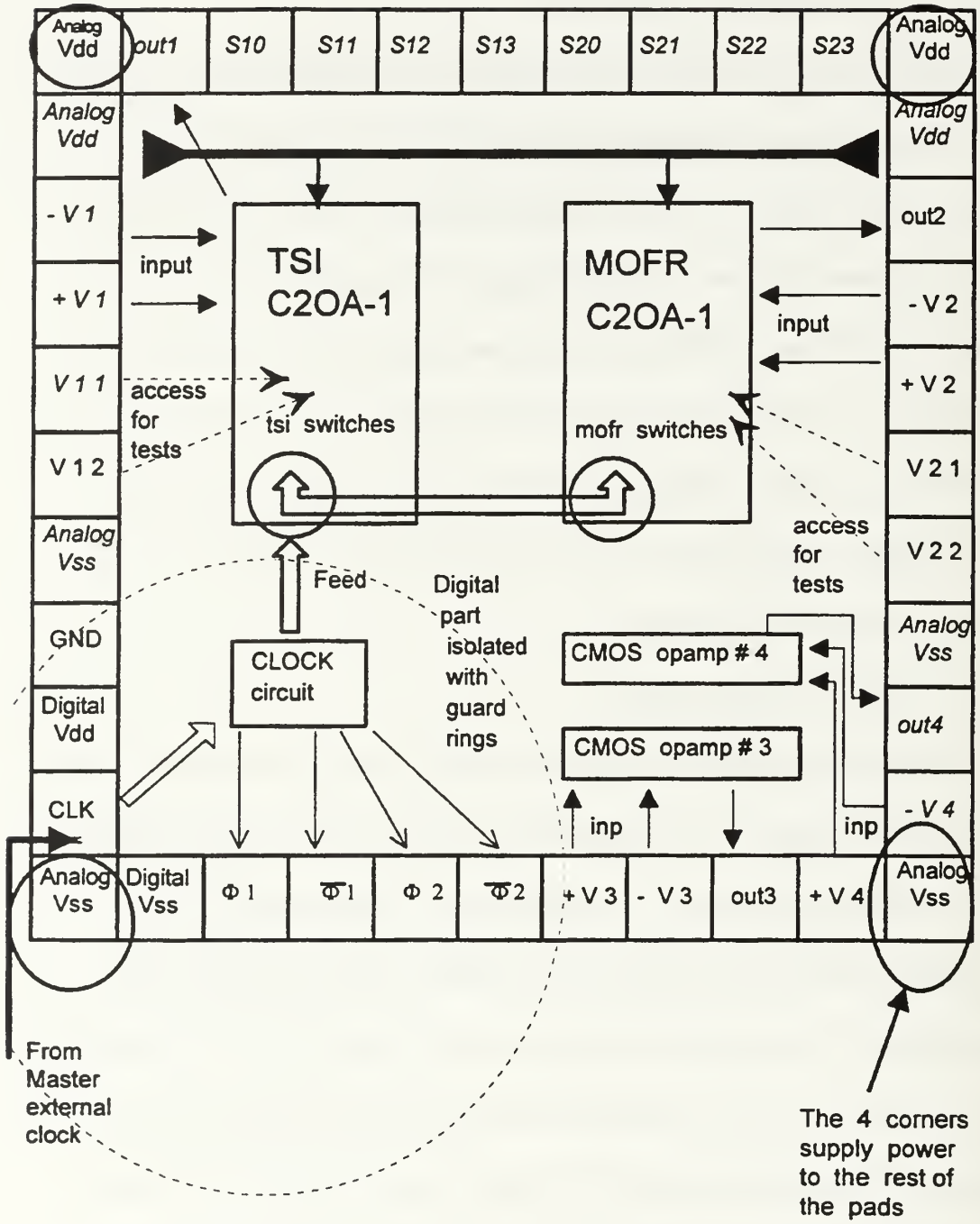


Figure 5.2 The floor plan of the test chip including the bond diagram. From Ref. (Anestis, 1994, p. 90)

These values were verified using the fabrication parameters and the relative size of the capacitors seen in Figure 5.1 (Anestis, 1994, p.144-146). The α in front of the Cr means that Cr's value can be multiplied by values from 1 to 16. If the actual values of the capacitors are close to the design values then by accessing the circuit at the test point the capacitance value should be from 6 to 24 picofarads. The actual value measured was about 12 picofarads. This value can be reached if, 1) α*Cr and Cn are in parallel, 2) the value for α is 6 and 3) the biphase clock is in the odd phase.

The test points used to access the capacitors correspond to pins 39 and 40 on the 40 pin chip. Another note, to operate properly Vss, Vdd and GND were supplied to the chip. The board is wired to provide a supply voltage of -5 volts to Vss and +5 volts to Vdd.

B. TEST CIRCUITRY

The circuitry used to test the capacitors is a simple low pass filter. The low pass filter is constructed using an LM 747 (twin op-amps in a single package with 14 pins) and two resistors (100 kΩ and 1MΩ) chosen to provide a gain of 10. The twin op amp LM 747 was chosen because initially it was thought there were two capacitors available on the test chip. One corresponding to the Toggle Switched Inverter (TSI) Composite Op-Amp (COA) and one corresponding to the Modified Open circuit Floating Resistor (MOFR) COA. Upon further testing of the chip it was determined that only the capacitor used in the MOFR COA design would be available for testing. A simplified schematic of the circuit is provided in Figure 5.4. The capacitor located on test chip #1 is placed in the low pass circuit such that it controls the pole corner frequency. The baseline response

is plotted as Figure 5.5. Figure 5.6 displays the baseline response from test chip #2. The entire circuitry is located on the same wirewrap board with input and outputs routed through BNC connectors into shielded coaxial cable available at the Linear Accelerator site. The photograph of the board in place in the linear accelerator is included as Figure 5.8.

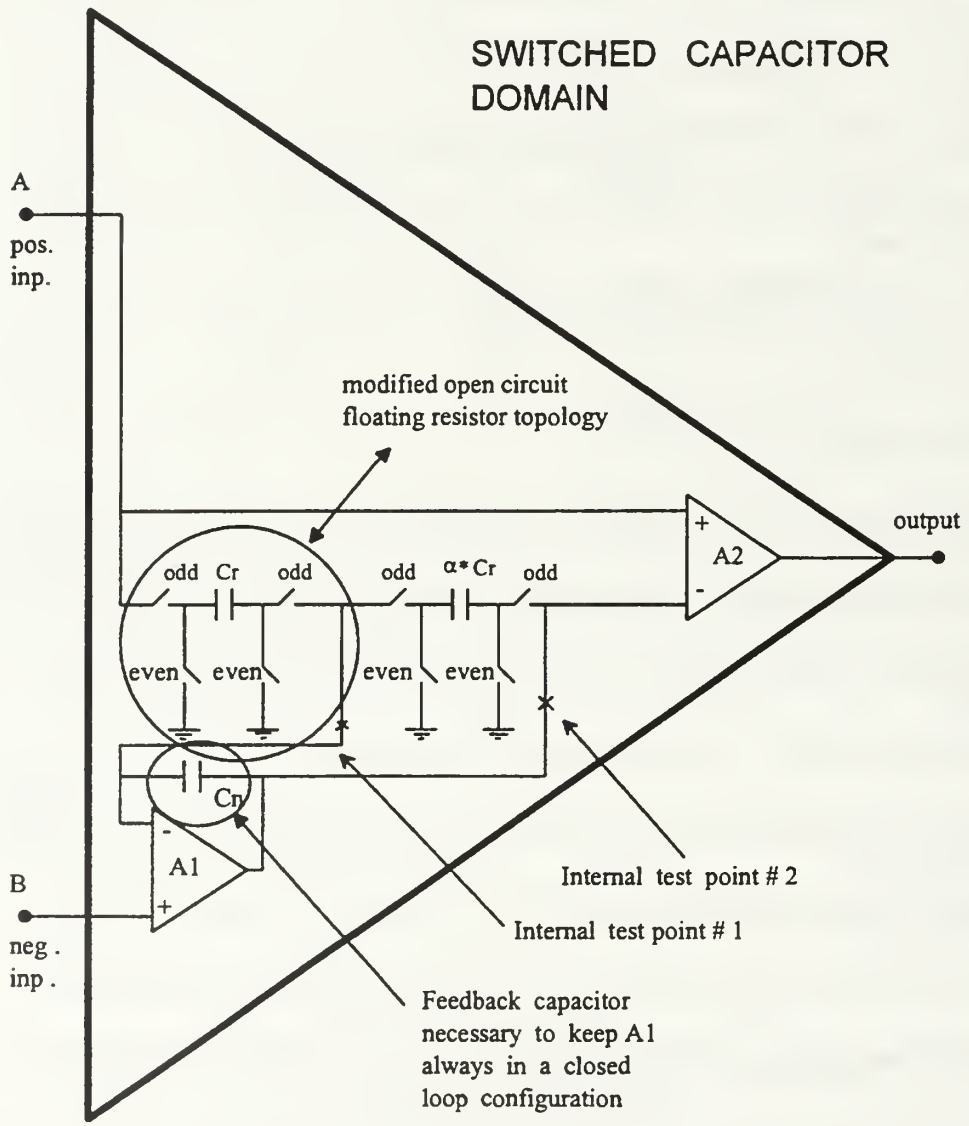


Figure 5.3 The simplified diagram of the composite op amp showing the location of the test points and the capacitors. From (Anestis, 1994, p. 52)

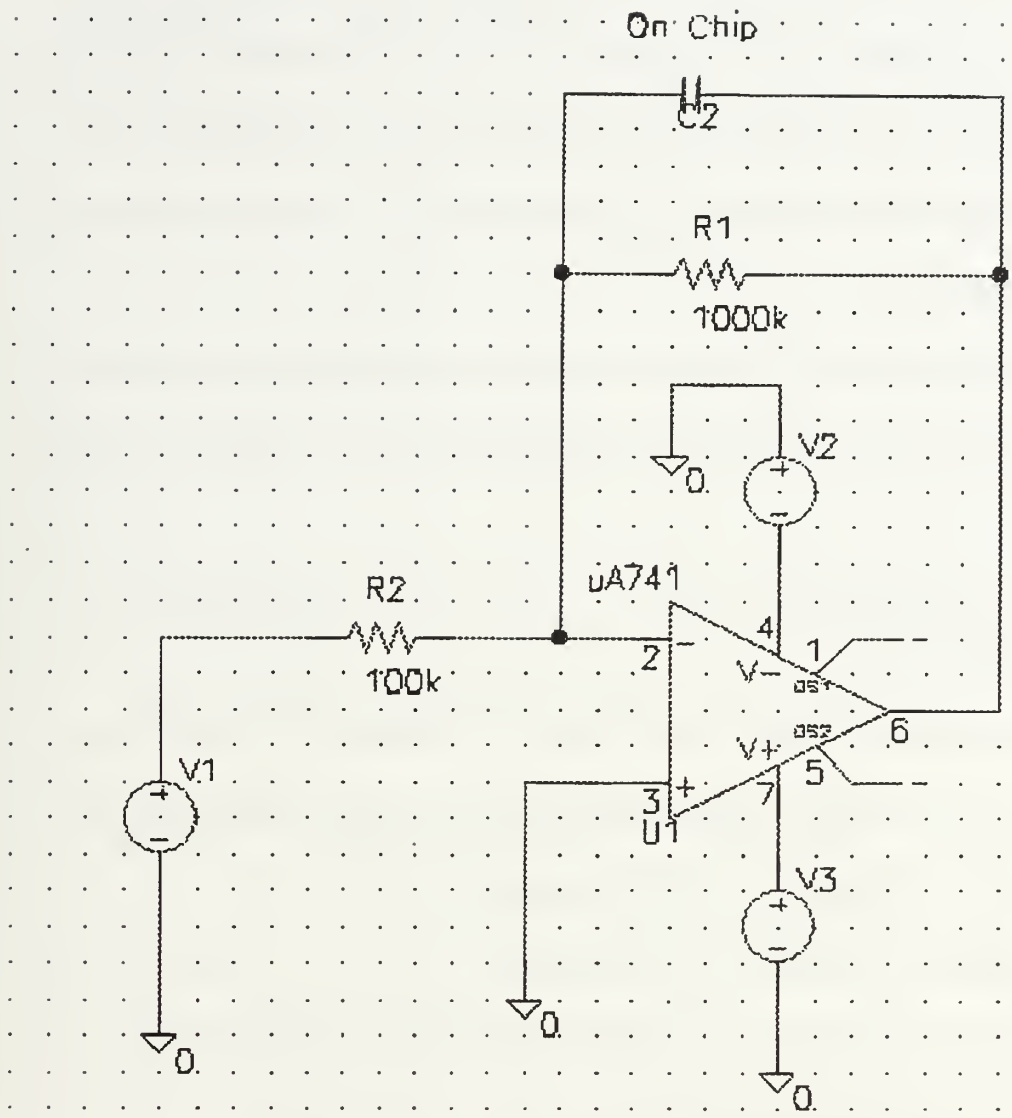


Figure 5.4 The Spice schematic representation of the low pass filter used in the radiation tests.

The signal input to the low pass filter is supplied from a Hewlett-Packard 3585B Signal Generator/Spectrum Analyzer (Figure 5.7). This piece of equipment allows the frequency to be swept from 20 Hz to 40 MHz. The frequencies of interest are much lower then 40 MHz. In most runs the frequency range used is 0.1 kHz to 20 kHz. The

output is plotted as frequency vs gain in dB. The baseline plots for both chips are found in Figures 5.5 (test chip #1) and 5.6 (test chip #2). In both baseline plots the marker has been placed at the 3 dB downpoint, the corner frequency of the low-pass filter. During the test runs the HP 3585B was placed in the LINAC control room to minimize personnel radiation exposure.

The frequency at the 3 dB point is the value used to calculate the capacitance (C). The equation used for this calculation is for a simple low-pass filter, Equation 5.1 (Sedra, 1991, p. 779).

$$C = (2\pi R_1 f)^{-1} \qquad 5.1$$

Where f is the 3 dB down frequency and R1 is the 1MW resistor in the filter circuit (see Figure 5.4). Using Equation 5.1 the calculated capacitances of the two chips are;

Test Chip #1 Capacitance = 12.556 picofarads

Test Chip #2 Capacitance = 12.575 picofarads

These values correspond well with the design value of 12 picofarads. This empirically verifies the assumptions made in section A. 2 of this chapter.

C. THE LINEAR ACCELERATOR

The source of radiation for this experiment is the Naval Postgraduate School electron linear accelerator (LINAC). The LINAC is located in the basement of Halligan Hall.

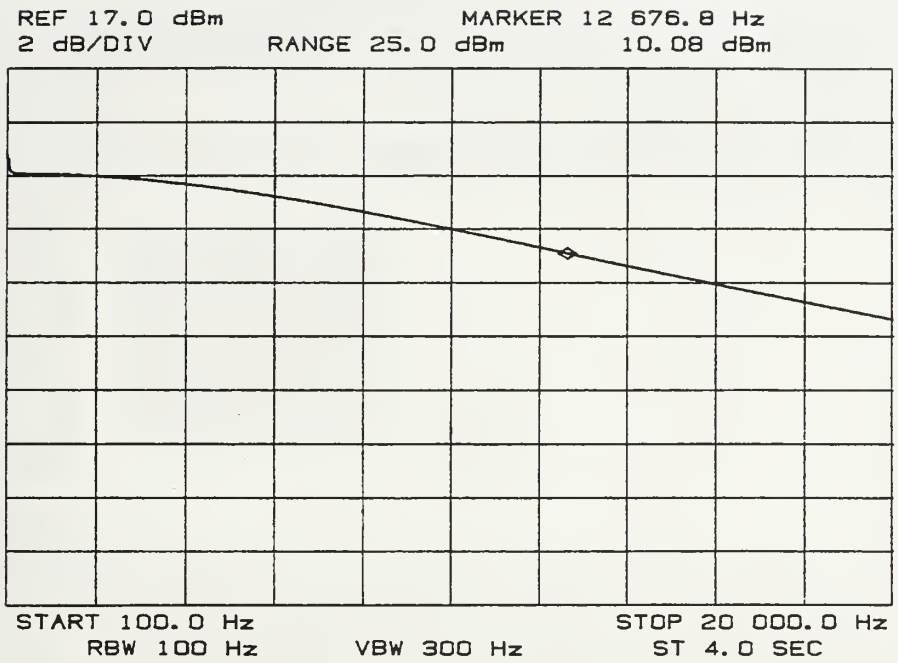


Figure 5.5 The baseline low pass filter curve for test chip #1.

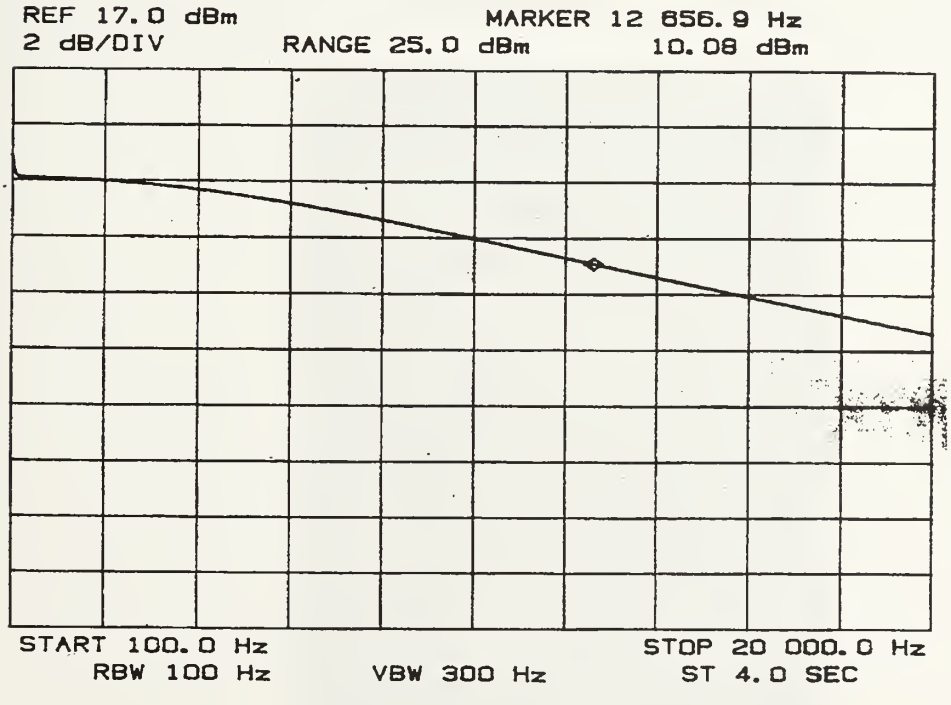


Figure 5.6 The baseline low pass filter curve for test chip #2

Figure 5.7 Photograph of the HP 3585B Signal Generator/Spectrum Analyzer.

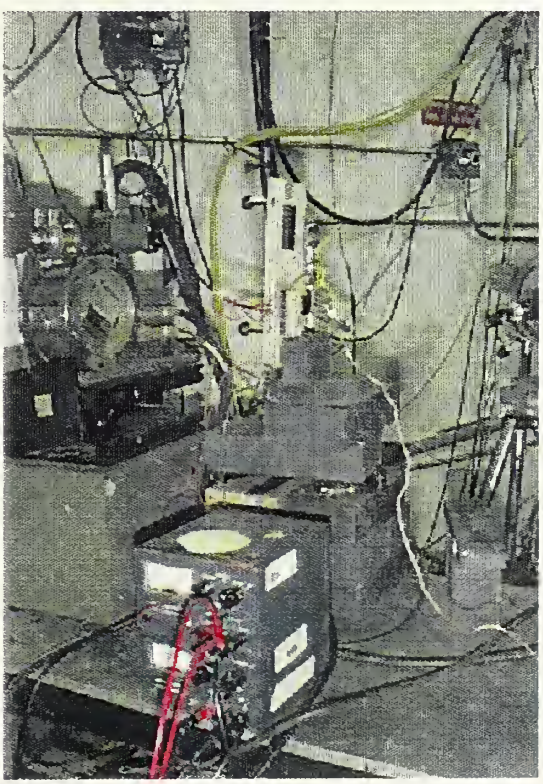


Figure 5.8 Photograph of the test board in place in the LINAC.

1. LINAC Overview

The NPS LINAC consists of three, ten-foot sub-accelerator sections. Each section is powered by a klystron amplifier delivering up to 22 Megawatts peak power. These klystron amplifiers are essentially miniature electron accelerators. They are cathode ray tubes which amplify the Radio Frequency (RF) signal needed to accelerate the electrons in the main sub-sections. The RF signal is generated by a trigger generator supplied to an RF driver operating at 2.856 GHz with a peak voltage of 6 kV. This RF signal is injected into the klystrons which amplify it using a pulsed 250 kV peak input. This high energy pulsed RF signal is focused using large electromagnets. The focused high energy RF is piped to the respective sub-accelerator sections via wave-guides. Figure 5.9 shows the three klystrons. (Barnett, 1966, p. 9)

The high energy RF signals are essentially waves. These high energy waves do for electrons what large ocean waves do for surfers. The electrons ride these high energy waves and in doing so are accelerated. The acceleration imparts energy to the electrons. This increases their energy level from 80 keV, at which they are injected, to the maximum rated level for the LINAC of 110 MeV. The source of these 80 keV electrons is an electron gun which is another cathode ray tube. The electrons enter the first accelerator section through a magnetic lens and pre-buncher. These help to focus the electrons and create the proper phase, so fewer electrons are lost upon entering the first section. Upon entering the first section, the electrons are accelerated in the first few inches to .8 or .9 times the speed of light. The remaining length of the accelerator (the rest of the first section and the remaining two sections) raises the electron energy level to

110 MeV. A photograph of the accelerator including the electron gun is found in Figure 5.10.

Since continuously maintaining a power output of 22 Megawatts is very difficult, due to temperature and input power constraints, the klystrons are pulsed at a rate of 60 Hertz with a pulse width of 3.5 μsec. This reduces the continuous rate of input power for each klystron to 4.62 kilowatts. This explains why the high energy RF is pulsed vice continuous.

The energy level of the electrons can be controlled in several ways. One way is by reducing the number of sub-accelerator sections being used. Each section raises the energy level by about 30 MeV. Thus for this experiment where low energy electrons were needed only the first section of the accelerator was used. This produced an electron beam of approximately 30 MeV. The actual energy level of the beam is controlled by the a collimator, a deflection magnet and energy defining slits. These are adjusted to control the energy level of the electron beam being produced. In this experiment the collimator and the slits were not used. The actual energy level is calculated by monitoring the voltage applied to the deflection magnet which deflects the beam at an optimum angle. For this experiment the voltage on the deflection magnet was 12 μvolts. This corresponds to an electron energy of 32 MeV. This energy is somewhat higher then normal electron energies found in space. Accepted values for electron energy levels in space are greater then 5 MeV with an average of 7 MeV (Schwank, 1994, p. II-5).

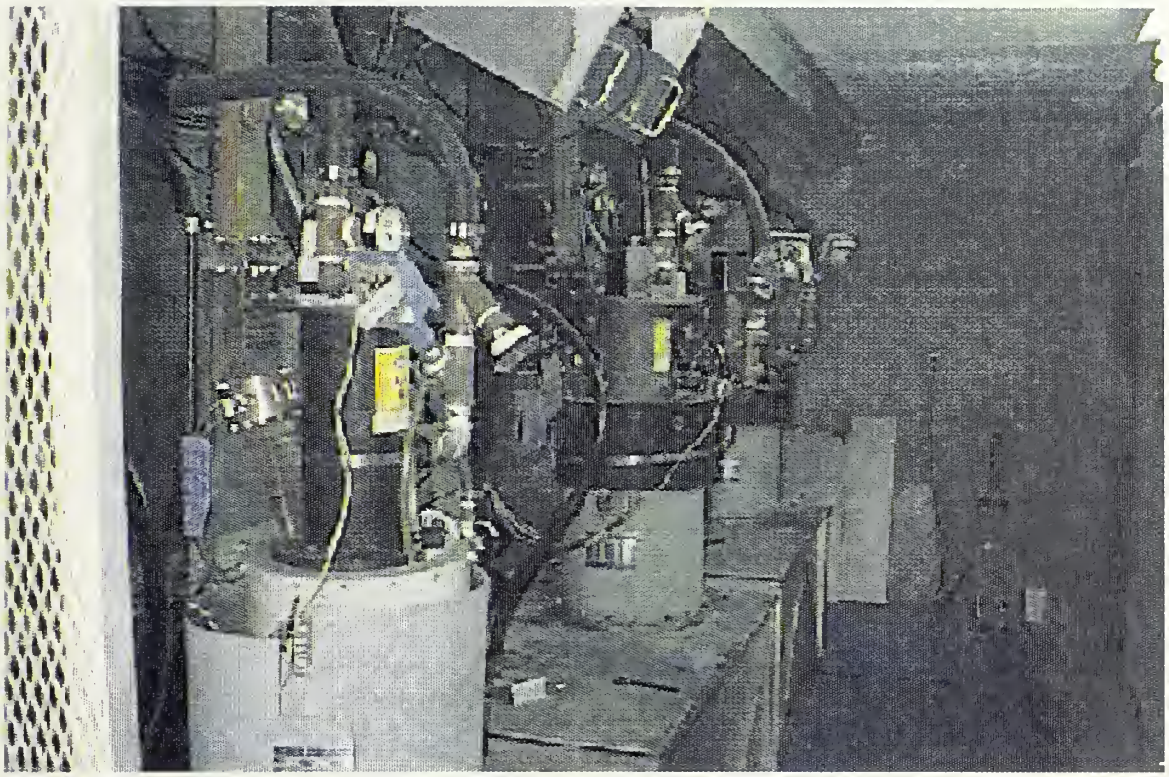


Figure 5.9 Photograph of the three main klystrons of the NPS LINAC.

Figure 5.10 Photograph of the electron gun and the sections of the NPS LINAC.

The deflection caused by the deflection magnets, places the beam into the target area containing the circuit board. This deflection, not only allows measurement of the electron beam energy, but also reduces the level of forward radiation caused by the electron beam in the accelerator sections. Figure 5.11 depicts the spatial layout of the LINAC area.

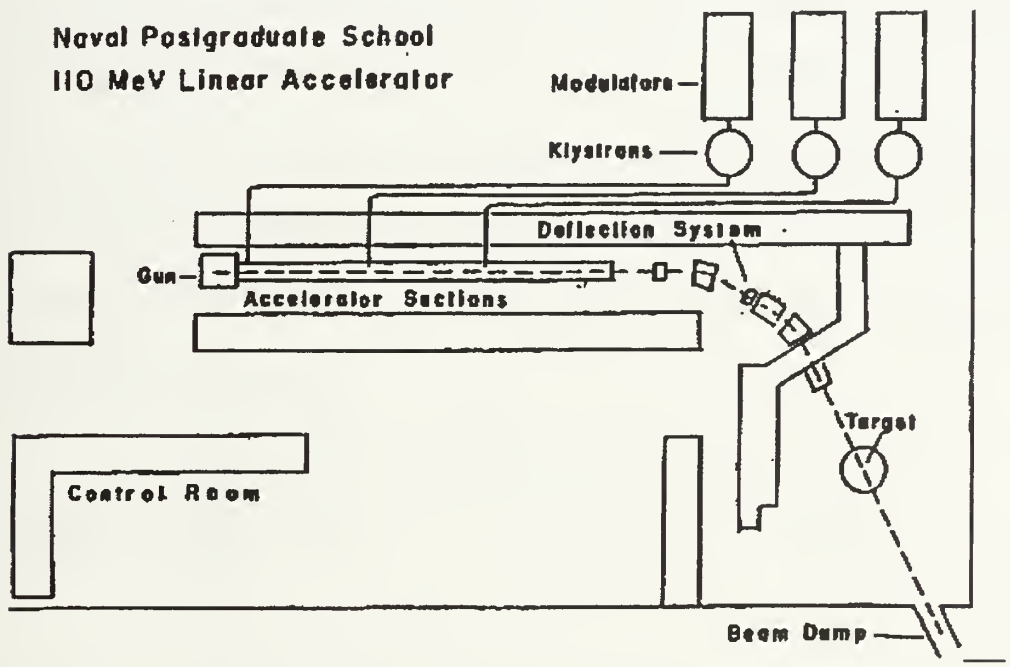


Figure 5.11 Spatial layout and major components of the NPS LINAC. From Ref. (O'Reilly, 1986, p. 73)

2. The Secondary Emission Monitor

The Secondary Emission Monitor (SEM) is used to determine the total number of electrons being delivered by the LINAC. This is called the fluence and has units of electrons/cm^2. The SEM is located at the end of the target chamber. As electrons pass

through it they create a current. This current is used to charge a capacitor of known value in the control room. The charge on the capacitor in volts is then linearly related to the fluence of the electron beam. As part of preparation for this experiment the SEM was calibrated.

SEM calibration is done in the following manner. A Faraday cup is used to catch all the electrons hitting the SEM. A Faraday cup is simply a lead lined conductor that absorbs all the electrons and converts them into current. A diagram of the set up is shown in Figure 5.12. Electrons hitting the charged plates in the SEM produce a current. The assumption is that all electrons in the beam that pass through the SEM are trapped in the Faraday cup and converted to current. The amount of time it takes to charge the 0.1 μfarad capacitors to the same voltage is recorded. The SEM efficiency (η_{SEM}) in percent is calculated using Equation 5.2.

$$\eta_{SEM} = \frac{time_{SEM}}{time_{FC}} \times 100 \qquad (5.2)$$

Where $time_{SEM}$ is the time to charge the capacitor attached to the SEM and $time_{FC}$ is the time required to charge the capacitor attached to the Faraday Cup. In actuality the same capacitor is used for both measurements. Two runs are made to determine the time to charge for each source. The efficiency is then used to calculate the total fluence (through the SEM) using Equation 5.3.

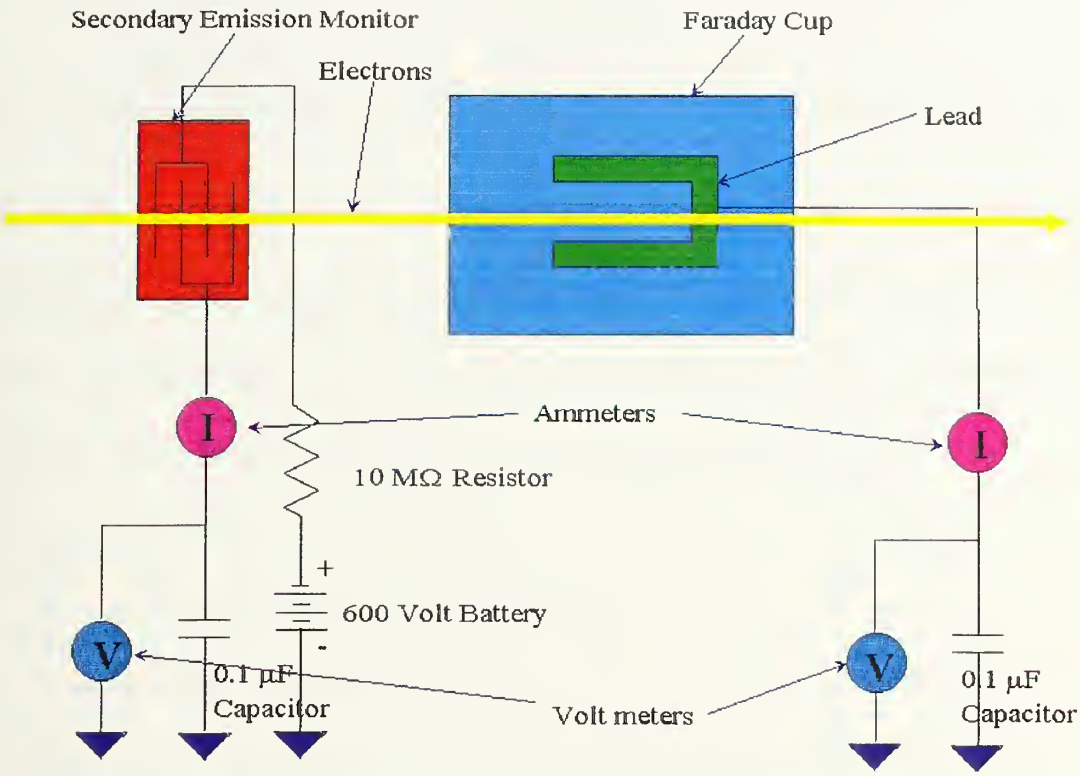


Figure 5.12 Setup for calibration of the Secondary Emission Monitor.

Figure 5.13 Photograph of the TLD reader.

$$N_e = \frac{VC}{\eta_{SEM} K} \qquad (5.3)$$

Where N_e is the number of electrons, K is a conversion factor from electrons to coulombs ($K = 6.25 \times 10^{18}$ electrons/coulomb), V is the charge on the capacitor and C is the value of the capacitor connected to the SEM. To find the actual fluence N_e (the number of electrons) must be divided by the surface area of the SEM to provided the proper units. Having done this calibration the charge on the SEM now reflects the fluence of an electron beam with a given intensity level and a certain electron energy level.

3. Correlation of Dose to SEM Charge

With the SEM calibrated to the number of actual electrons passing through it, another means must be employed to relate total dose to the charge on the SEM. This is done using a Thermal Luminescent Dosimeter (TLD).

a. The Thermal Luminescent Dosimeter

The TLD is a device used to measure total dose radiation. It consists of a small Calcium Fluoride chip impregnated with Manganese impurities. When exposed to ionizing radiation electrons and holes are produced and trapped at metastable energy levels in the forbidden gap. These levels are created due to the Manganese impurities. The number of filled levels is proportional to the total dose absorbed. The total dose is measured by heating the TLD chip. When heated, the trapped electrons are released and these electrons recombining with holes produce light. The intensity of this light is proportional to the total dose received by the TLD. (Kerris, 1992, p. I-13)

There are some limitations to this process. One of these limitations is the maximum allowed dose on the TLD. The maximum dose allowed for this TLD is 1 kRad (Victoreen, p. 3-14, 1986). However, the levels needed to simulate a space environment are much higher then this. In fact the levels used for this experiment were above 2.4 MRads (1MRad = $1x10^6$ Rads) A photograph of the instrument used to read the TLD's can be seen in Figure 5.13.

b. Application of the TLD

A process was developed by the LINAC staff to correlate the charge on the SEM with the dose received by a TLD. A TLD is placed at the location of the device to be tested in the electron beam. The LINAC is turned on for a very short period of time, since the TLD saturates at levels above 1000 Rads. After each exposure the TLD is read and the dose is plotted versus the charge accumulated on the SEM. The plots can be seen in Figures 5.16 (day #1, 5 November, 1996) and 5.17 (day #2, 6 November, 1996). The SEM accumulated charge is related to a specific dose using a linear relationship. This provides for calculating the total dose received by the chip. These calibration runs are done both days due to the changing electron beam profile.

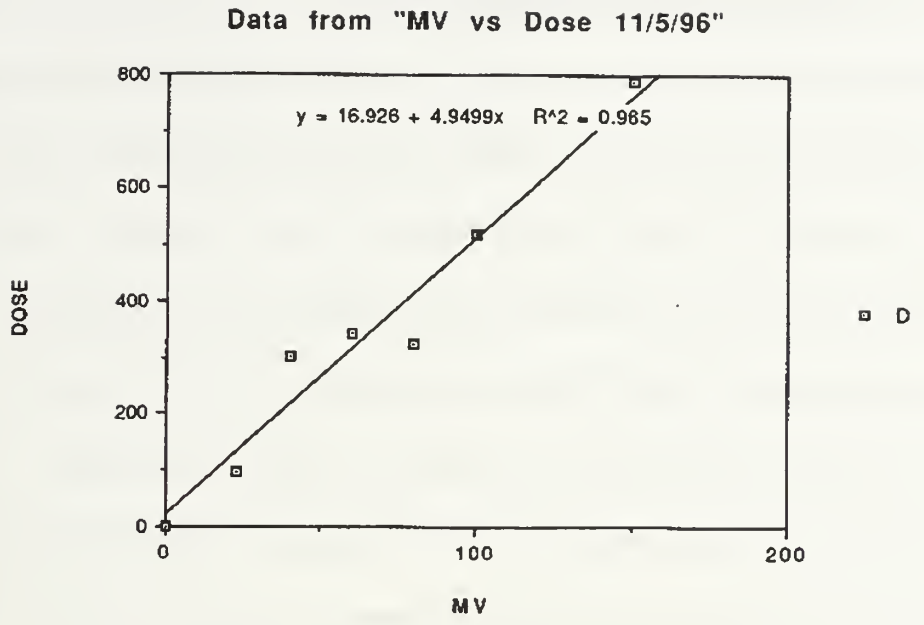


Figure 5.14 The relationship of TLD Dose (Rads) to SEM charge (mV) for day #1 (11/5/96).

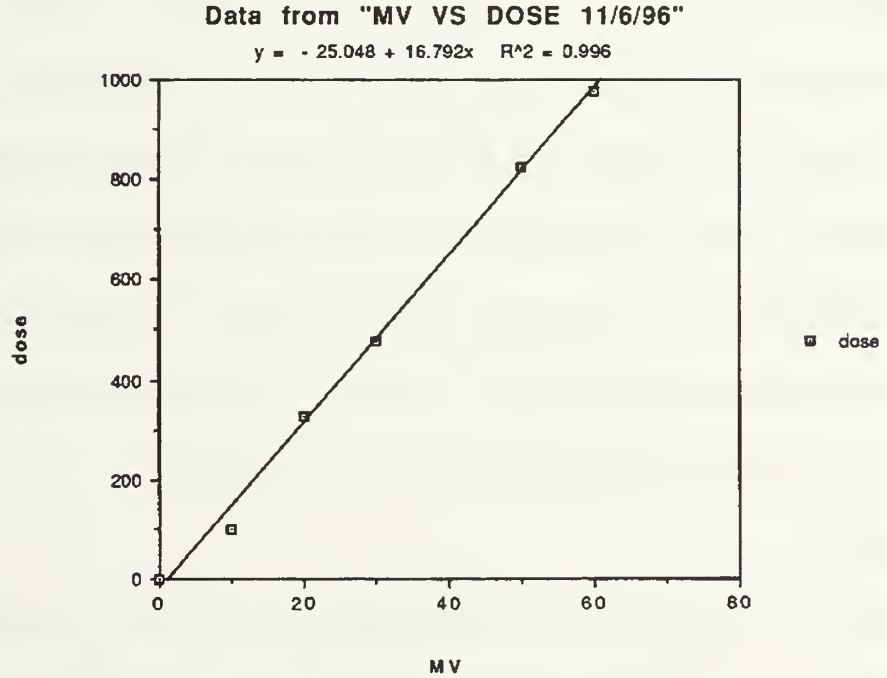


Figure 5.15 The relationship of TLD Dose (Rads) to SEM charge (mV) for day #2 (11/6/96).

4. Measurement of the Electron Beam Profile

The final aspect of the LINAC taken into account is the electron beam profile. The profile of the beam is its intensity cross section. This was determined back in 1967 to have a shape resembling a flat topped hill (see Figures 5.16 and 5.17) (Nelson, 1967, p. 28-29). For this experiment some verification of actual beam intensity is done using electroluminescent paper (paper coated with the same phosphorescent material used to coat the inside of television picture tubes). This paper glows brighter with a higher intensity of electrons. A live video camera is set up to continuously monitor the paper which is placed over the location of the test chip. The beam is turned on and focused onto this paper. The intensity of the light created by the paper is analyzed using an image analyzer program. The lights are extinguished in the target area for this procedure. The paper's glow reflects the actual intensity of the beam. The light intensity is fed into a computer and the computer creates a 3D representation of the actual beam intensity. The exact intensity is difficult to determine using this method however, the relative intensity can be seen. Figures 5.18 and 5.19 are the 3D representations of beam intensity for day 1 (5 November, 1996) and day 2 (6 November, 1996) respectively. The beam intensity is relatively uniform across the area of the chip. The lines of lesser intensity seen in the pictures are actually pencil marks that mark the center of the target chip.

D. SUMMARY

This chapter covers the actual setup of the experiment. There are several details which are covered briefly. The actual experiments involve operating the LINAC while

the filter response was observed. The data obtained is tabulated in Appendix B, Experimental Data, the results of this data are discussed in the next chapter.

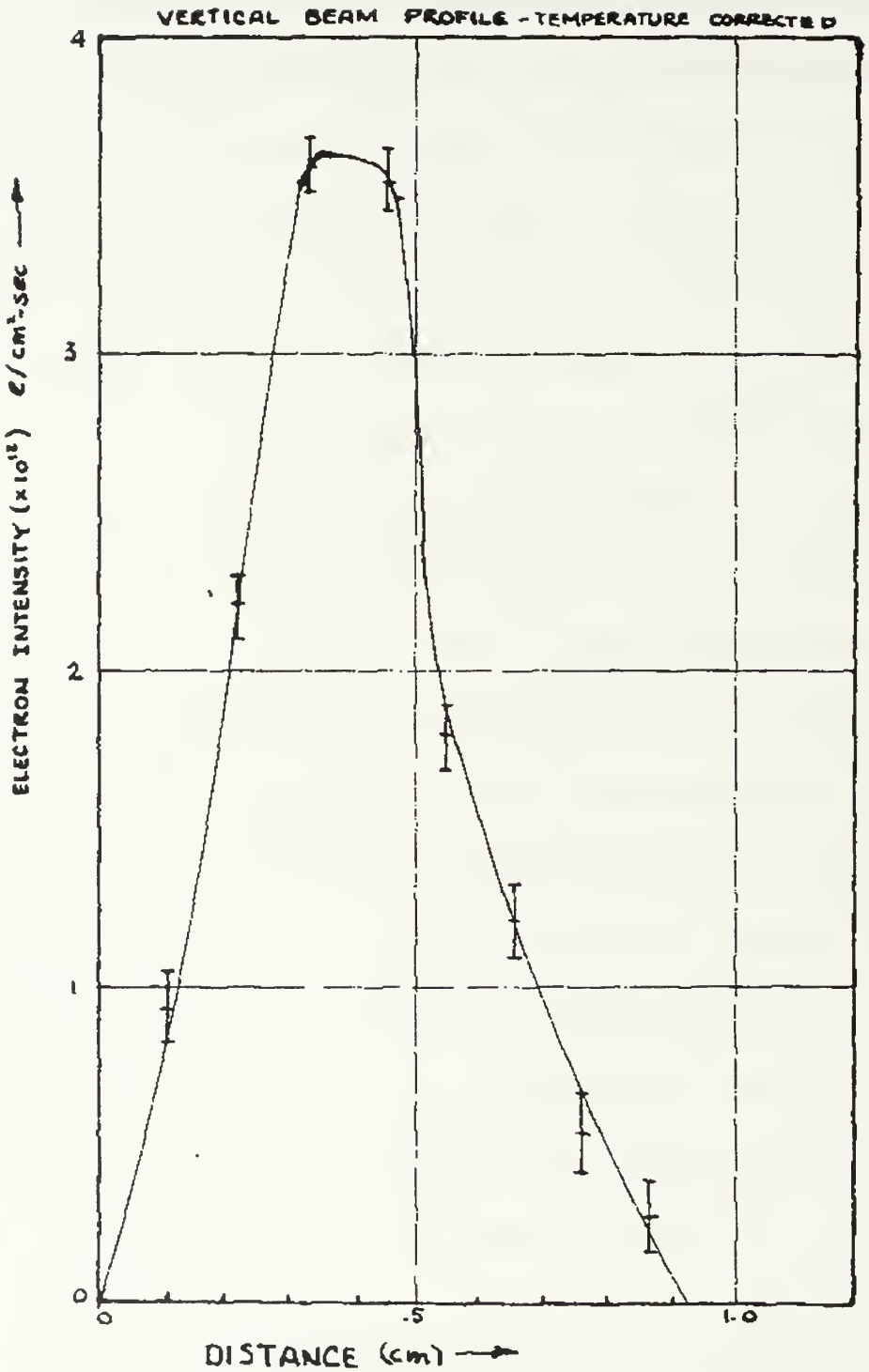


Figure 5.16 The vertical beam profile plotted as fluence vs position. From Ref. (Nelson, 1967, p.31).

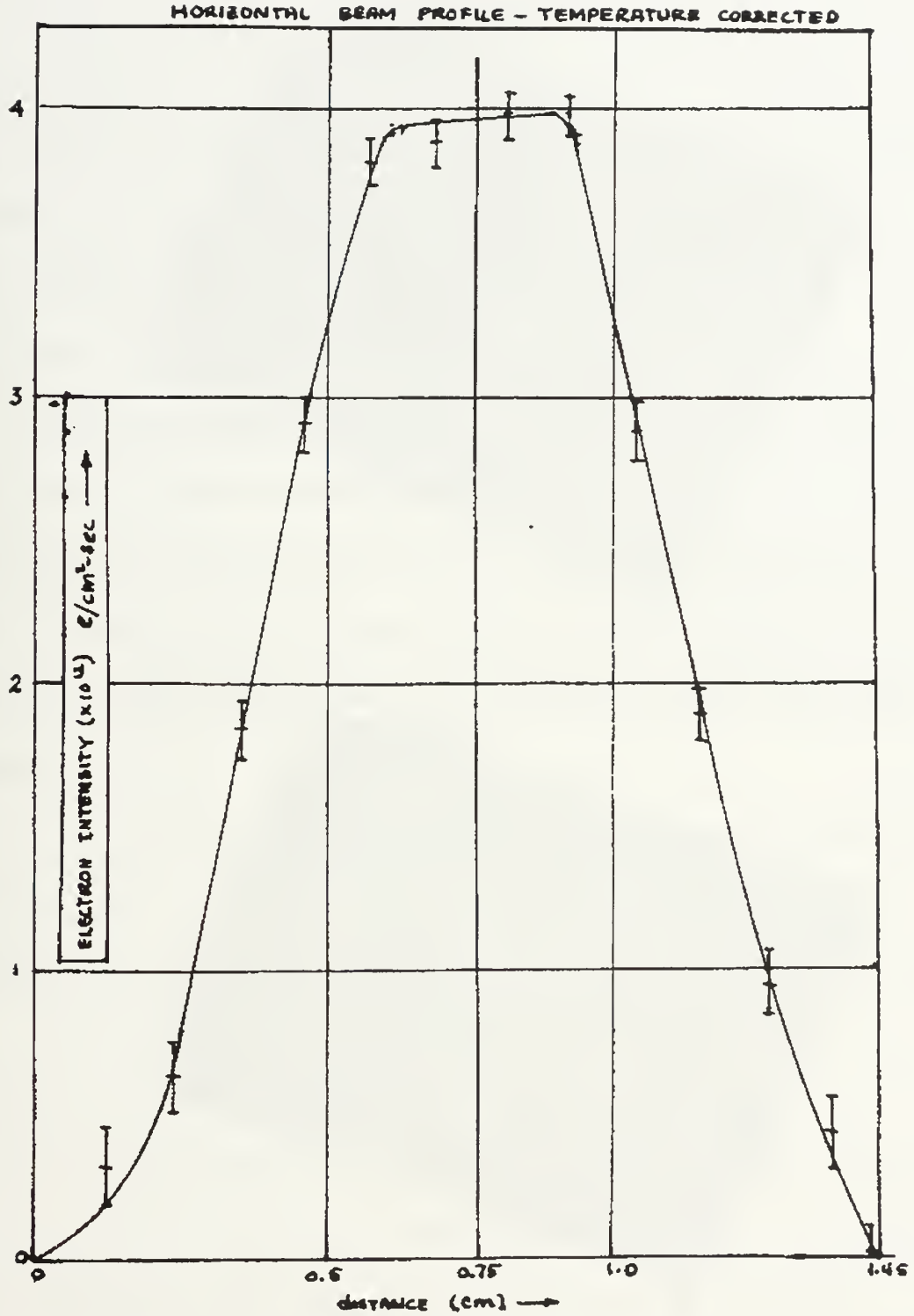


Figure 5.17 The horizontal beam profile plotted as fluence vs position. From Ref. (Nelson, 1967, p.30).

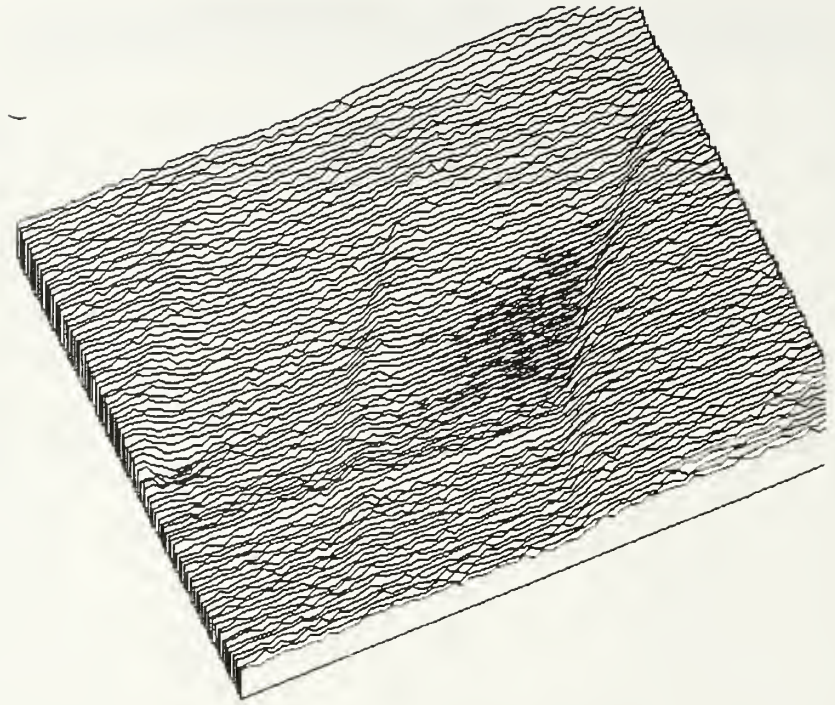


Figure 5.18 The beam profile in 3D from run 1 (5 November, 1996).

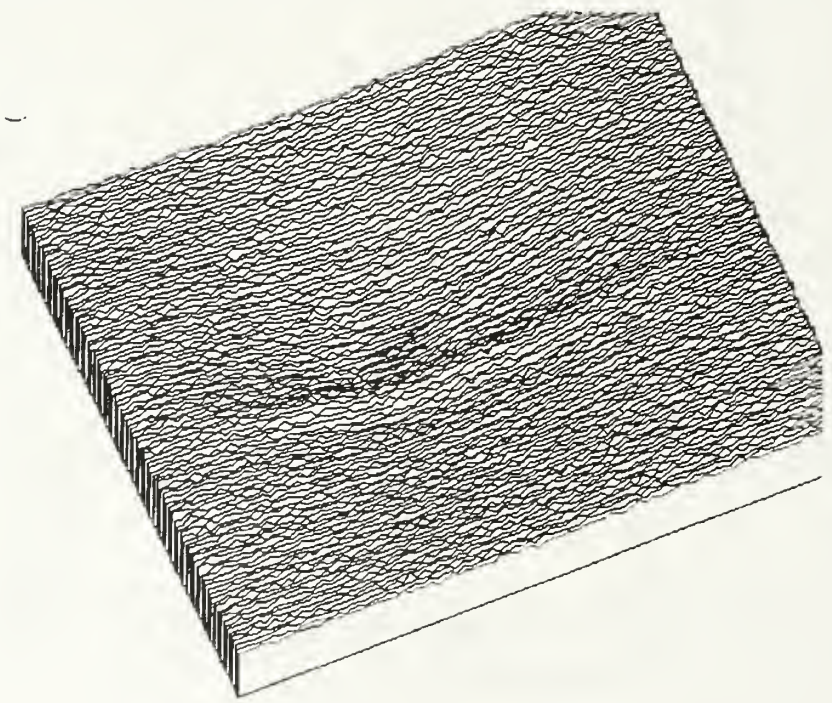


Figure 5.19 The beam profile in 3D from run 2 (6 November, 1996).

VI. RESULTS

A. RUN ONE

The first run was completed on 5 November, 1996. The chip used was designed by Rapheal Anestis (1994). The chip was marked as #3. This chip also had a white sticker with all the pins identified. Prior to starting the radiation run a baseline plot was made (Figure 5.7). From this baseline plot the initial capacitance was calculated.

Before the run began the two initialization procedures described in Chapter V were completed. First, the beam intensity determination was done (Figure 5.18). Then, the SEM charge to dose measurements were taken (Figure 5.14). During the beam intensity procedure the beam was focused on the location of the 40 pin chip socket. Care was taken to maintain the same position of the board when the chip was inserted at the beginning of the run.

In this run there was a thermocouple placed between the chip and the socket. The readout was placed in the "hold" mode and did not accurately display the temperature during the run. This problem was rectified on run two by using a different thermocouple.

The accelerator was started with the chip in place at 10:35. Initially it was decided to use small increments of dose. This was due to the earlier experiments conducted by Abrahamson (1995) in which he reported chip failure on similar chips at a total fluence of 2.08×10^{13} electrons/cm^2. However, upon further review of Abrahamson's data it appears that the failures took place from 2×10^{15} to 6x10E^{15}. These values correspond well with the values for fluence observed in this run.

Initially the LINAC was operated in short bursts providing 500 to 1500 Rads per burst. After about ten burst type operations the accelerator was left on and the SEM charge and time to charge were recorded continuously. The three dB downpoint values were taken only when a noticeable shift occurred in the frequency location. These values are tabulated in Appendix B. The chart that reflects these values can be seen in Figure 6.1. This chart also contains the data from run number two.

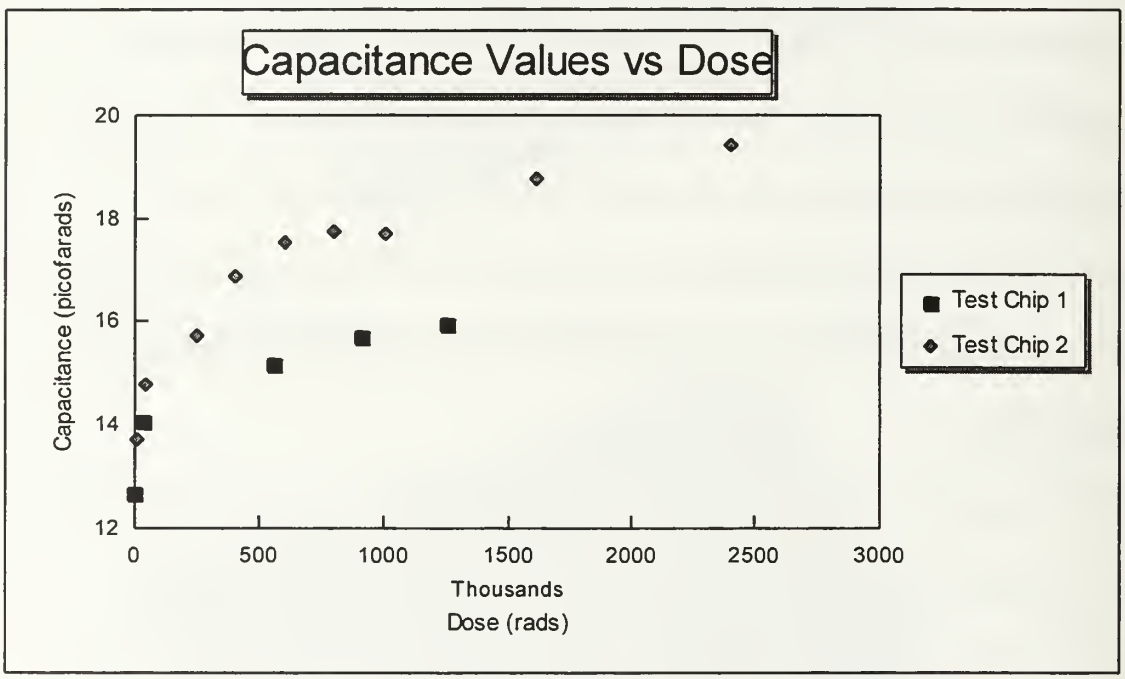


Figure 6.1 The chart depicting capacitance vs dose for both test chips.

As can be seen the capacitance values tend to increase with increasing dose. This result corresponds to the results reported by Abrahamson (1995, p.81). The data used to calculate the dose as a function of SEM charge for both days is also included as Figure 6.2. This same information can be found in Figures 5.14 and 5.15.

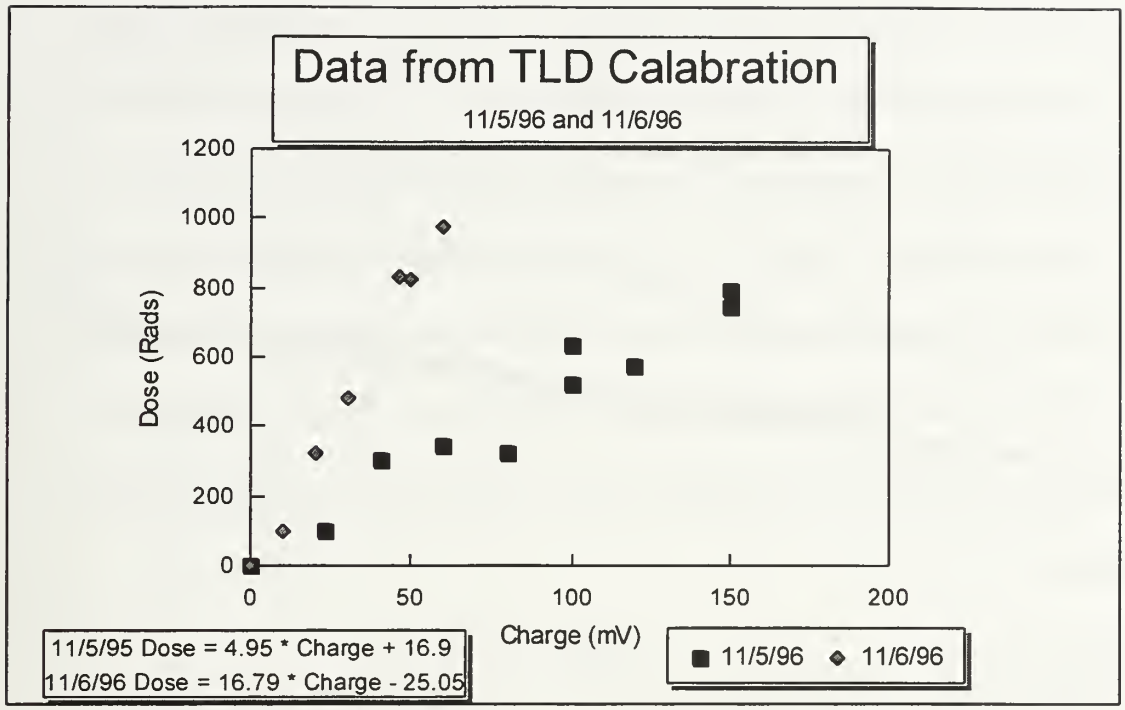


Figure 6.2 Chart displaying the dose to SEM charge relationship for both days.

At 2,552 seconds into the run, the LINAC electron beam was turned off and the LM 747 op-amp chip was replaced. There was concern that the op-amp in the LM 747 chip having been exposed to the radiation might actually fail causing erroneous results. Lead shielding was placed around this chip to help prevent radiation effects on it. This shielding can be seen in Figure 5.8. The LM 747 was replaced prior to the beginning of each run. For run one it was replaced at the 1.7 MRad point (2,552 seconds). When the electron beam was reinitiated there was no significant change in output.

An unexplained phenomena occurred when the electron beam was extinguished. The response slowly shifted down. The final value of the shift without the electron beam can be seen in Figure 6.3. This plot displays two traces the upper trace at approximately -45.5 dBm is the trace associated with the chip after the beam was turned off. The second

noisier trace at -65 dBm is the trace from the circuit with all power removed from both the LM 747 and the test chip. The unexplained phenomena took place when the electron beam was restarted. At this point the filter response actually returned to where it was prior to securing the beam. Figure 6.4 is a dual plot of the filter response at the beginning of the radiation run and at the completion with a total dose of 2.66 MRads (a fluence of 2.182×10^{15} e/cm^2). The upper curve is the initial curve and the lower one is the response at completion. Once again when the electron beam was removed the response decayed to that of Figure 6.3.

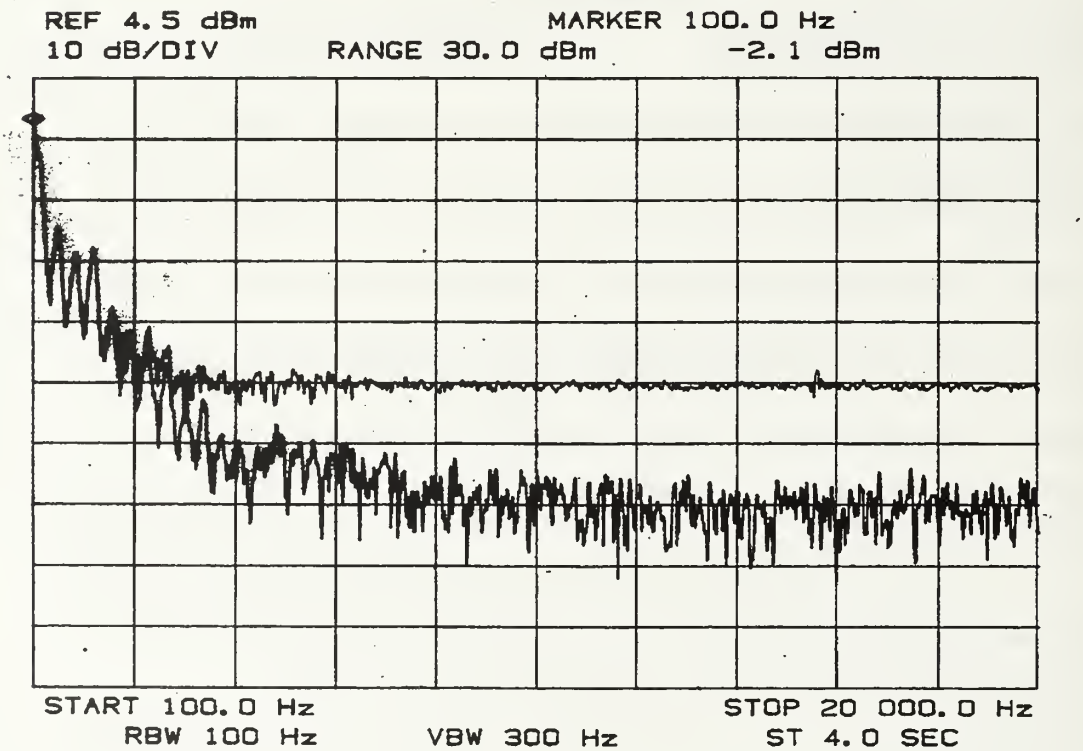


Figure 6.3 The plot of the filter response when the electron beam was extinguished at the completion of run one (dose = 2.66 MRads).

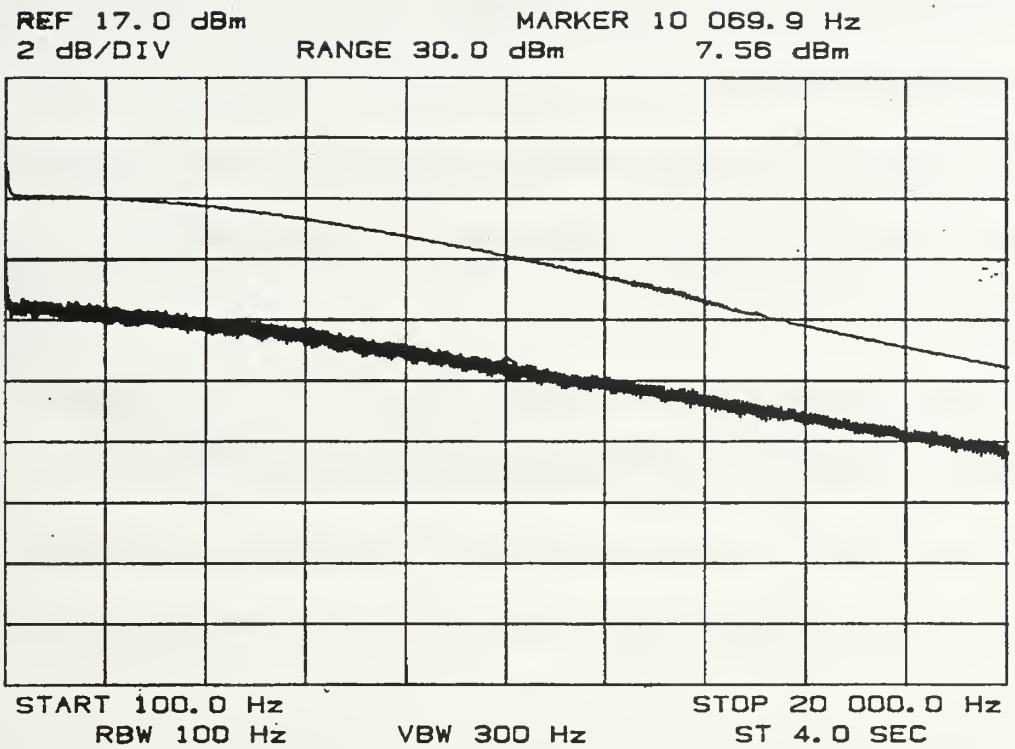


Figure 6.4 The plot of the initial response (upper curve) and the final response (lower curve) corresponding to a dose of 2.66 MRads with the beam energized.

B. RUN TWO

The second run took place on 6 November, 1996. In this run a second chip identical to the first was used. It was labeled #2.

Once again, as in day one, the initialization runs were done. The results of the beam intensity run is found in Figure 5.19. The results of the TLD dose to charge runs are found in Figures 5.15 and 6.2 (the tabulated results are found in Appendix B).

In this run the thermocouple functioned properly. The tabulated temperature results are found in Appendix B. The temperature initially rose from 50° C to 57° C and then lowered and stabilized at 50° C. It was determined that temperature had little effect on the results of this experiment.

The beam was turned on at 1:54 pm. During this run the beam was left on and the SEM charge values and times were recorded continuously. The readings were recorded for the 3 dB downpoint. These values are tabulated in Appendix B. Figure 6.1 illustrates the capacitor to dose relationship. Once again the capacitor value increases with total dose increase.

The same unexplained phenomena took place when the beam was extinguished at approximately 2.215 MRads. The filter response decreased dramatically. Figure 6.5 illustrates the response when the beam was turned off. The upper plot at approximately -30 dBm is the response of the filter with no beam. The lower noisy trace is the output with no power supplied to the chip or the LM 747. As with test chip one when the beam was restarted, the filter response returned to where it was before it was secured. Figure 6.6 is a plot of the initial response and the final response at 2.4 MRads. The upper curve is the initial response, the lover curve is the final response.

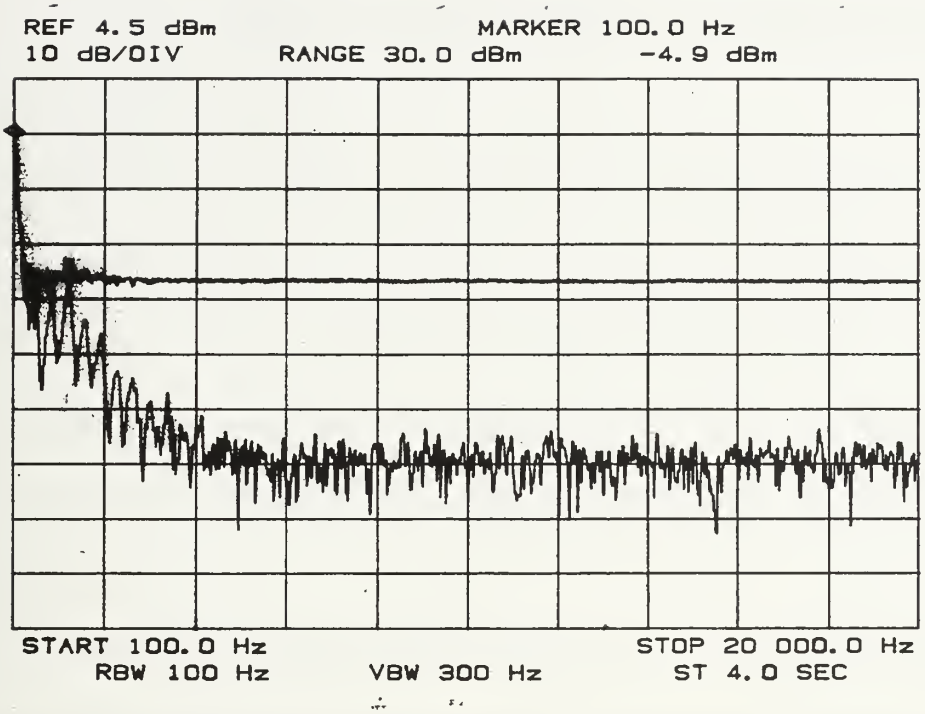


Figure 6.5 The filter response plot when the electron beam was extinguished at the completion of run two (dose = 2.4 MRads).

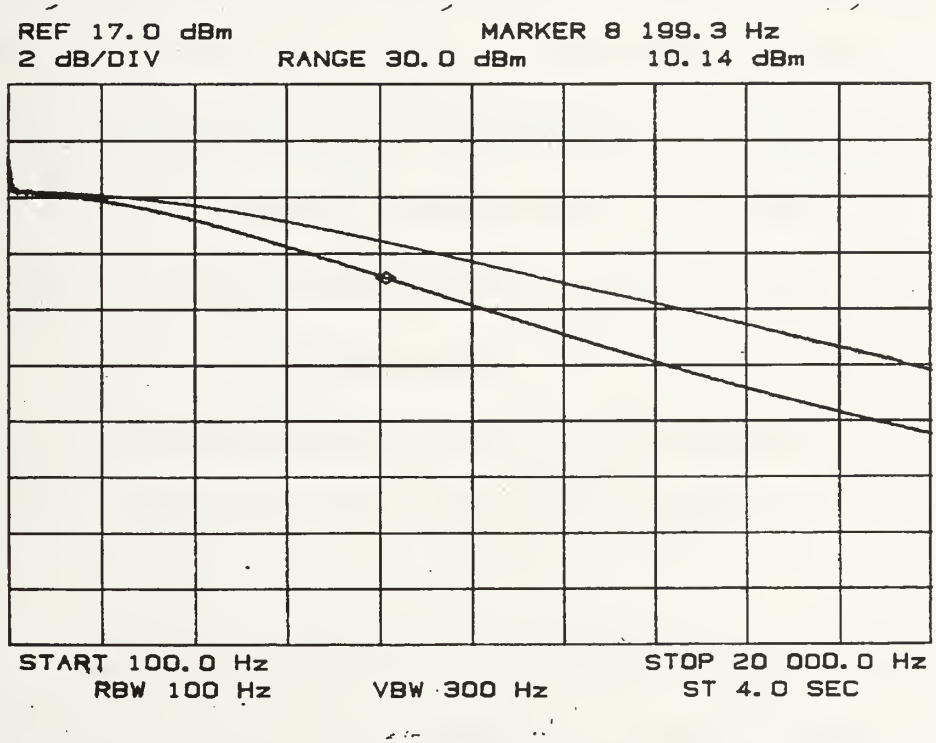


Figure 6.6 The plot of the initial response (upper curve) and the final response (lower curve) corresponding to a dose of 2.4 MRads with the beam energized.

VII. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

This thesis is a follow on to some unique research done here at NPS. The investigation of radiation effects on MOS VLSI capacitors while they are under a radiation flux. The results verified the previous research by Abrahamson (1995). The initial goal of this work was to add to the data base of knowledge concerning radiation effects on MOS VLSI analog components specifically the capacitor. This goal has been accomplished.

Previous work in the 1980's irradiating MOS VLSI capacitors yielded results which differed from the results received here. In 1984 Winokur irradiated MOS capacitors constructed from a p-type chip. His capacitor had a capacitance of 78.5 picofarads and it received a maximum of 1 MRad of dose at a dose rate of 240 Rads per second. He measured the capacitors after several runs by analyzing the high frequency and low frequency quasi static capacitance-voltage (C-V) (Winokur, 1984). His results, in Figure 7.1, indicate that as dose increases capacitance decreases. In both NPS theses the results indicate that as dose increases capacitance increases. The capacitance change was observed by the degradation of the low pass filter output discussed in the previous chapters. These results indicated that the actual capacitance was going up (see Figure 6.1).

The anomalies seen during the experiments included the following; after both chips failed they recovered when they were placed back in the radiation source, the

electron beam. The second chip tested recovered to its baseline response after 24 hours. To help explain these observations more testing is necessary.

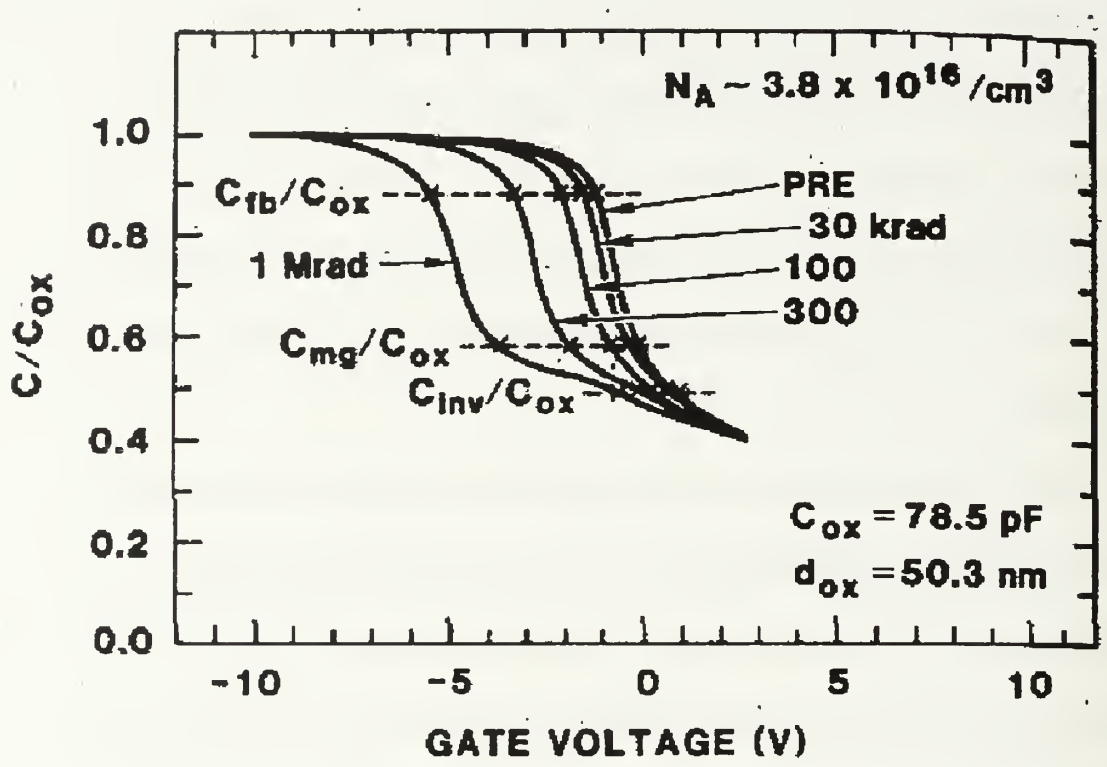


Figure 7.1 C-V curve which shows decreasing capacitance with increasing radiation dose. From Ref. (Winokur, 1984, p. 1454)

B. RECOMMENDATIONS

The data recorded in these radiation experiments are very promising. The use of Commercial Off The Shelf (COTS) parts for space vehicles is very plausible due to the cost savings. In-situ radiation testing is an excellent way to observe how radiation interactions affect the devices under test. This in-situ type of testing can certainly be applied to other areas including, solar cells, radiation hardened components or other types of integrated circuitry, to name just a few.

There are several follow on projects in this area. The chip which is being fabricated (see Appendix A) can be used for further testing. More runs can be made to determine if the energy level of the electrons create a different response. The LINAC at NPS is available for these types of radiation tests.

APPENDIX A. THE SPECIALTY CHIP

A. OVERVIEW OF THE SPECIALTY CHIP

The purpose of this appendix is to discuss the construction of a specialty chip designed to be used in the type of testing conducted in this thesis. An MOS VLSI chip was designed as a project for the VLSI design class at Naval Postgraduate School (EC 4870). The design for this chip was completed using the Cadence computer aided design suite. The Integrated Circuit Front to Back (icfb) tool in this package is well suited for this type of design. Prior to the design described here all chips submitted for fabrication to the MOSIS fabrication process from the Naval Postgraduate School were done using the MAGIC design tool. The initial chip design was completed in March of 1996. This design had to be modified to conform with MOSIS standards. There was a great deal of time spent in the modification process and the final design was not submitted until August of 1996. This did not allow for the chip to be fabricated in time for use in this thesis. This appendix is to describe how the chip was designed as an aid for follow on work in the area of in-situ MOS VLSI capacitor testing.

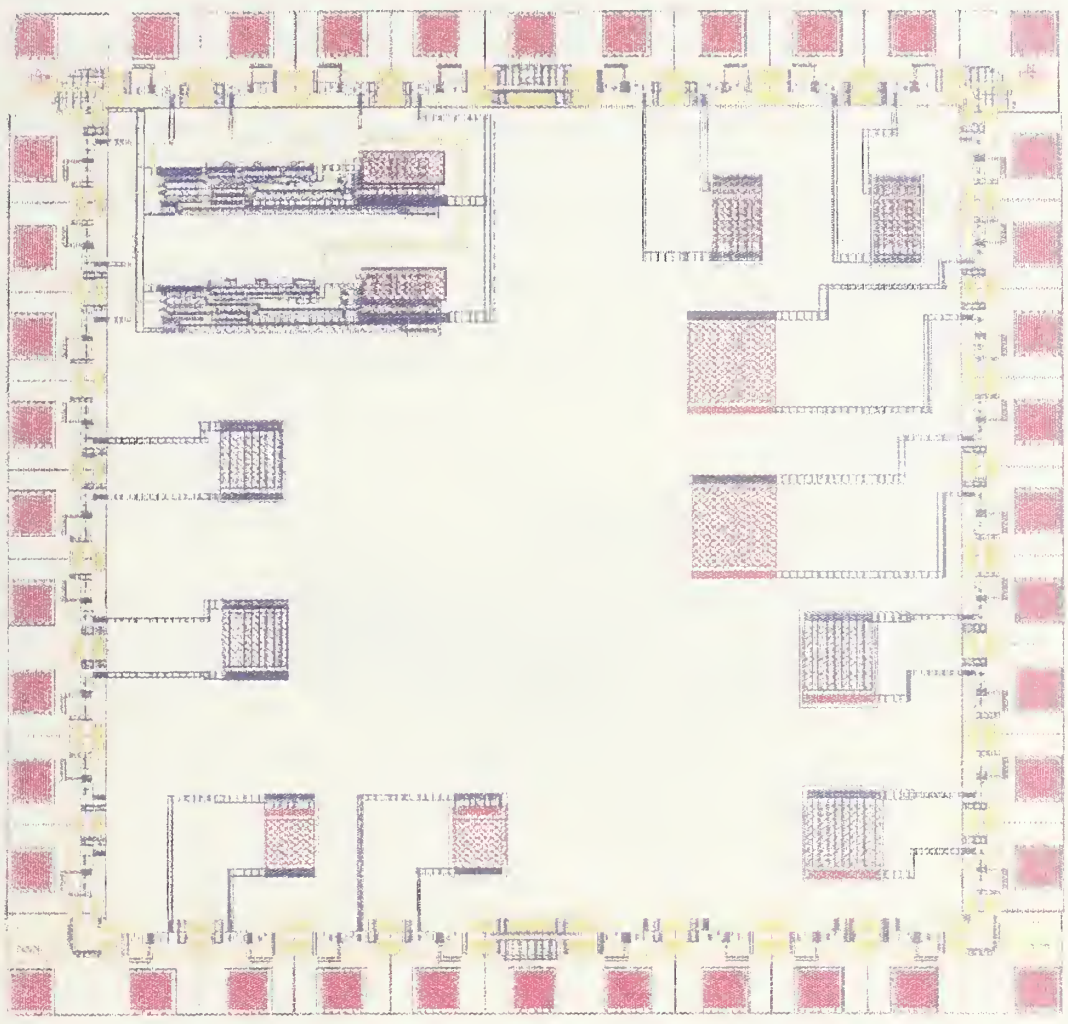


Figure A.1 The lay out of the MOS VLSI capacitor chip.

1. Capacitor Design

The Chip is designed with 10 discrete capacitors. There are five different designs with two capacitors for each design. The chip also contains two op-amps designed by another student in the EC4870 class. These op-amps have nothing to do with the capacitor design but could be used to construct filter circuits if desired. The layout of the chip is found in Figure A.1. Figure A.2 is a ghost chip floor plan. This figure labels all the capacitors and the pins corresponding to each capacitor. An explanation of each capacitor follows.

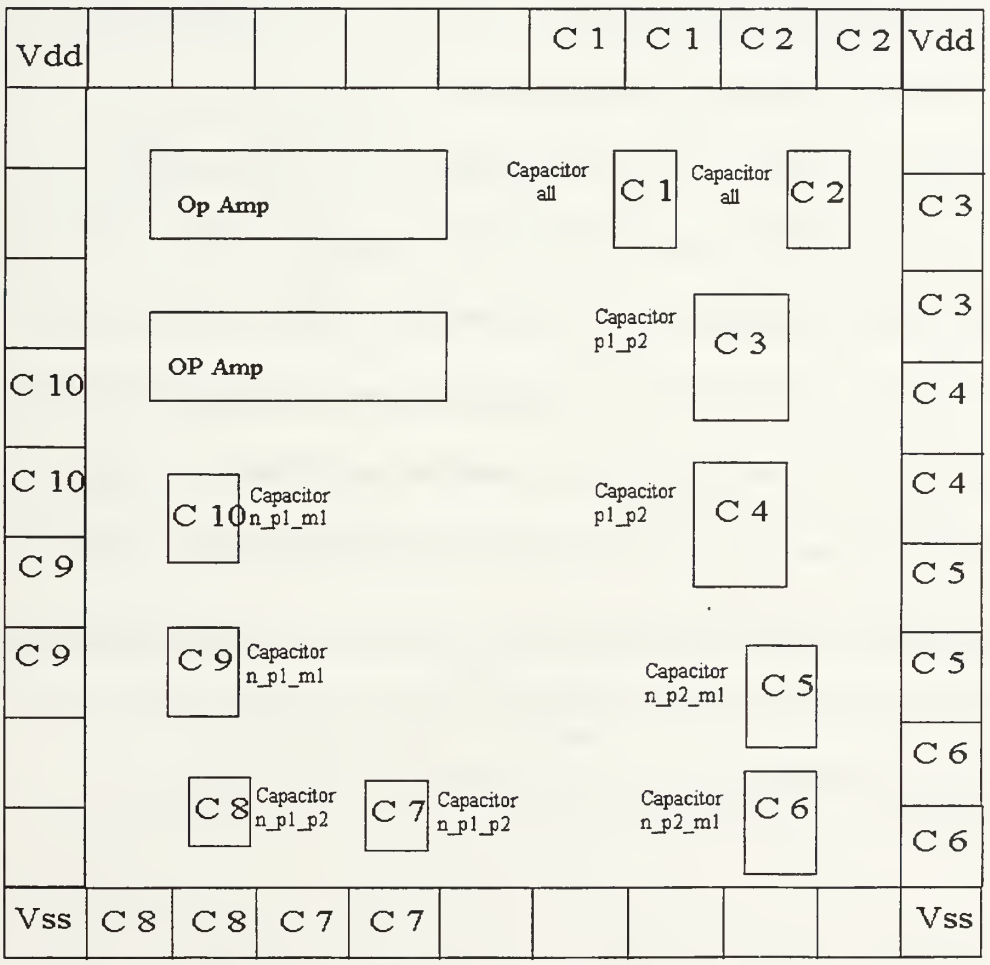
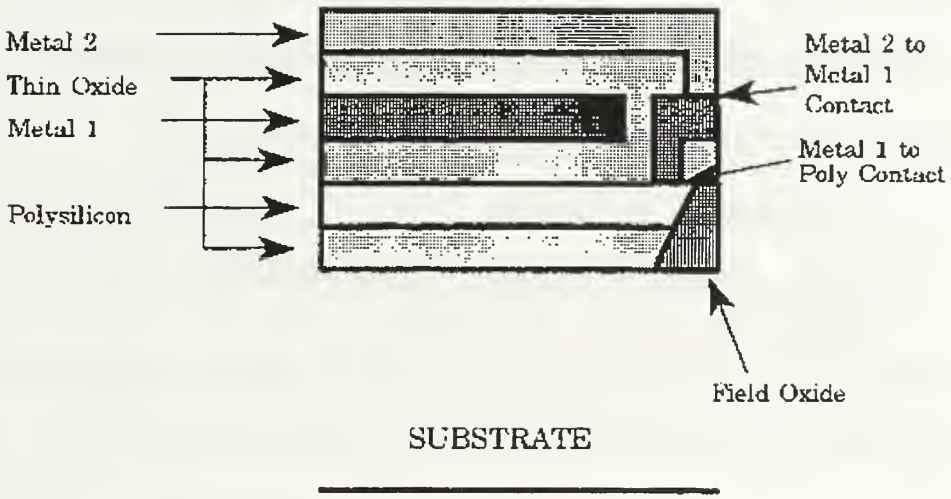


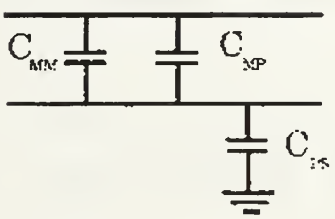
Figure A.2 The ghost chip floor plan for the MOS VLSI capacitor chip.

a. The Cap_all Capacitor

This capacitor is constructed of all the different layers available, hence its name. The bottom is n+ followed by poly_1, then poly_2, next metal_1 and finally metal_2. A cross sectional view of Cap_all is found in Figure A.4. Between each layer of active material is a layer of SiO_2 which acts as the dielectric for the capacitor. The thickness of these SiO_2 layers depends on the process being used. A report from MOSIS should accompany the chip when it arrives. This report should reflect both the thickness of the dielectric SiO_2 layers and the thickness of the active layers. The location of these two capacitors is in the upper right-hand corner of the chip as seen on Figure A.2. They are labeled C 1 and C 2. The size of these capacitors is 100μm x100μm. These dimensions produce a capacitance of 13.74 picofarads. This value is determined using the results from a "MOSIS Parametric Test Results" document dated 2 May, 1996. This report contains capacitance parameters in attofarrads/μm^2. Using these values and the dimensions of each type of material used the, capacitance value can be calculated. The design of each capacitor is based on the values from this report. This type of capacitor yields the largest capacitance for the smallest area. This is due to the additive effects of the parallel capacitors. An example of this can be seen in Figure A.3. In this example only three layers are used but it is clear that the capacitances are added in value. All of the other types of capacitors are designed with this additive effect in mind.



Circuit Diagram



Compensating Capacitance

$$C_C = C_{MM} + C_{MP}$$

C_{MM} Metal 2 to Metal 1 Capacitance

C_{MP} Metal 1 to Poly Capacitance

C_{PS} Poly to Substrate Capacitance

Figure A.3 Illustration of a three layer MOS Capacitor. From Ref. (Silvernagel, 1993, p. 35)

b. The Cap_n+_p1_p2 Capacitor

This capacitor also has a high capacitance to size ratio. It is constructed starting with a layer of n+ then a layer of poly_1 followed by a layer of poly_2. Once again each layer is separated by a layer of SiO_2 as a dielectric. Figure A.5 contains the

cross sectional view of this capacitor. Its size is also 100μm x 100μm. This yields a capacitance of 12.99 picofarads. These capacitors are located in the lower left hand corner of the chip as seen in Figure A.2. They are labeled C 7 and C 8.

c. The Cap_p1_p2 Capacitor

This capacitor is created using just a layer of poly_2 over a layer of poly_1. The chips created by Anestis (1994) and tested in this thesis are constructed this way. Most MOS parallel plate capacitors fabricated today utilize this poly on poly capacitor design. The Cap_p1_p2 capacitor has the lowest capacitance to area ratio. The cross section view is Figure A.6. The area of this capacitor is 176μm x 176μm. The actual capacitance is 14.03 picofarads. These capacitors are located on the right side of the chip in Figure A.2. They are labeled C 3 and C 4.

d. The Cap_n+_p1_m1 Capacitor

This capacitor is constructed on a layer of n+ followed by a layer of poly_1 and capped by a layer of metal_1. The cross section is found in Figure A.7. The capacitor size is 125μm x 125μm. This equates to a capacitance of 13.81 picofarads. These capacitors are located on the right hand side of the chip directly under the op-amps. They are labeled C 9 and C 10.

e. The Cap_n+_p2_m1 Capacitor

This capacitor is created on top of a layer of n+ followed by a layer of poly_2 capped with a layer of metal_1. It has a capacitance of 14.6 picofarads with a size of 140μm x 140μm. The cross section is in Figure A.8. These capacitors are located in the bottom right hand corner of the chip Figure A.2 and labeled C 5 and C 6.

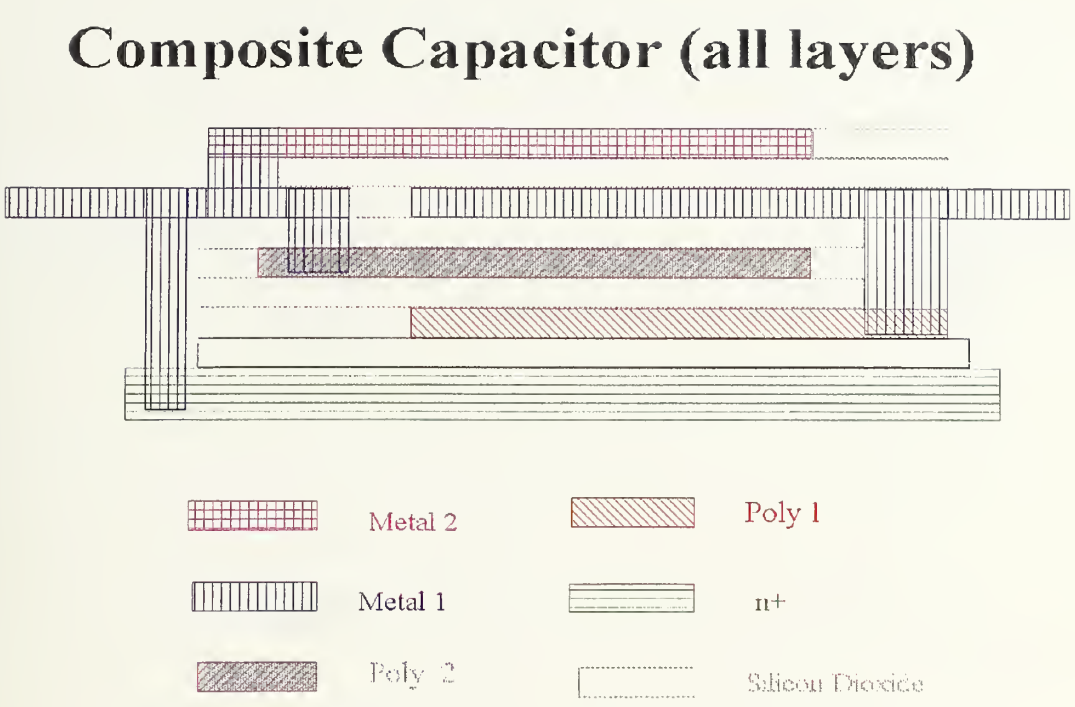


Figure A.4 The cross sectional view of the Cap_all capacitor.

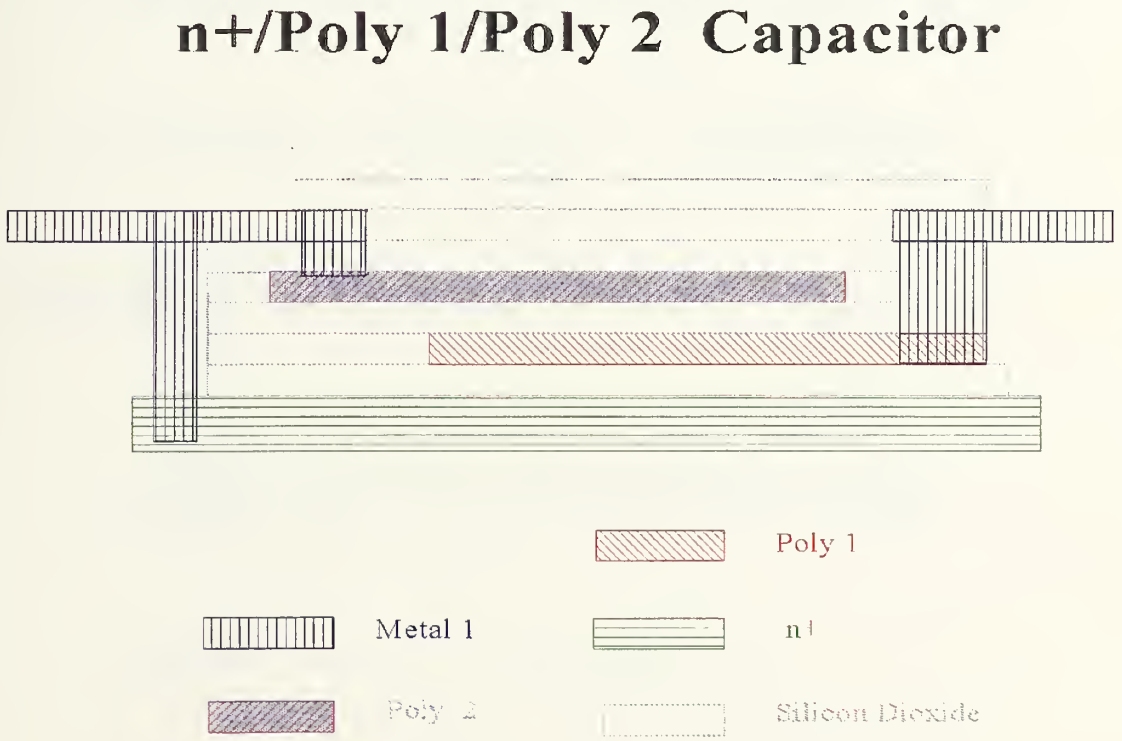


Figure A.5 The cross sectional view of the Cap_n+_poly1_poly2 capacitor.

Poly 1/Poly2 Capacitor

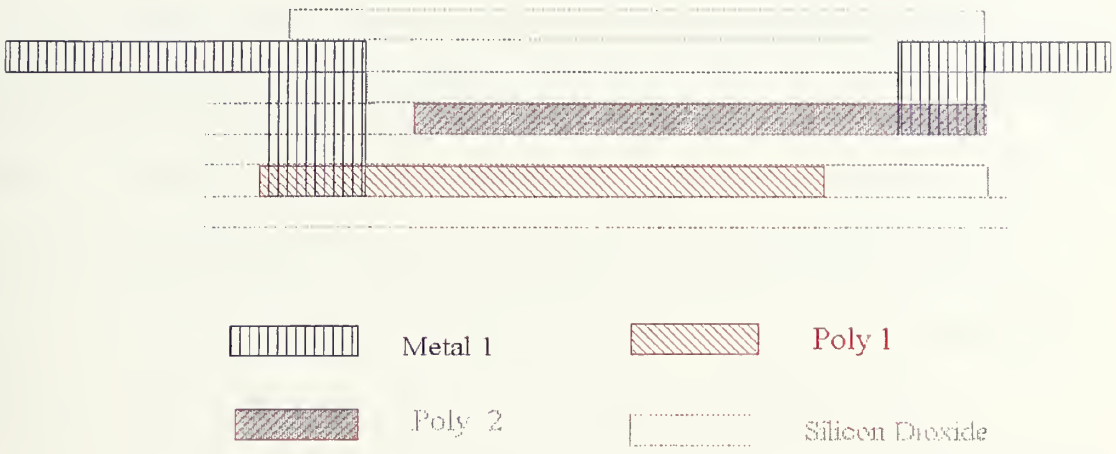


Figure A.6 The cross sectional view of the Cap_poly1_poly2 capacitor.

n+/Poly 1/Metal 1 Capacitor

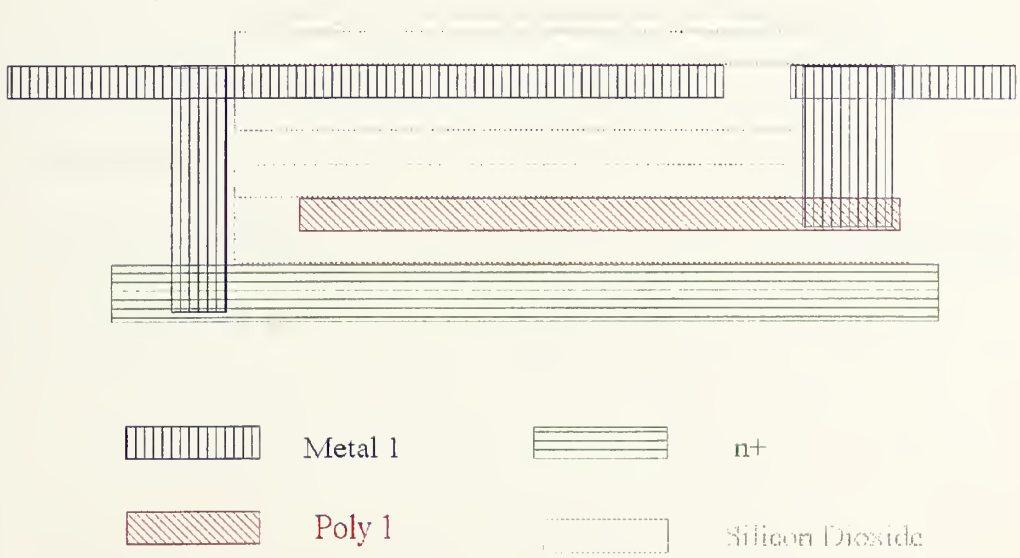


Figure A.7 The cross sectional view of the Cap_n+_poly1_metal1 capacitor.

2. Capacitor Commonalties

All five of these capacitor designs have some commonalties. The first item is their shape. All of the shapes listed above were square. As can be seen in Figure A.1 they are not actually square. This is due to the connections used between layers. The MOSIS files that were provided with the design tool contained some specific connection instances. The different layers were connected using these provided connectors. The area used by the connections causes the capacitors to appear rectangular. These connections will no doubt add to the capacitances for each design. Each cross sectional figure gives a quantitative relationship as to the types of connections used.

Another communality shared by all the capacitors was the routing metal used. In all cases metal_1 was used to route the capacitors to their respective pads. This was possible due to the simplistic design of the chip which did not require any leads to cross enroute to the pad ring. In the routing of the op-amps it can be seen that both metals were necessary.

Another common trait mentioned above is all the active layers are separated by a layer of SiO_2. This acts as the dielectric for the capacitors.

B. SUMMARY

This chip was designed to be used in a test such as the one performed in this thesis. This appendix is to aid follow on research that may use this chip.

n+/Poly 2/Metal 1 Capacitor

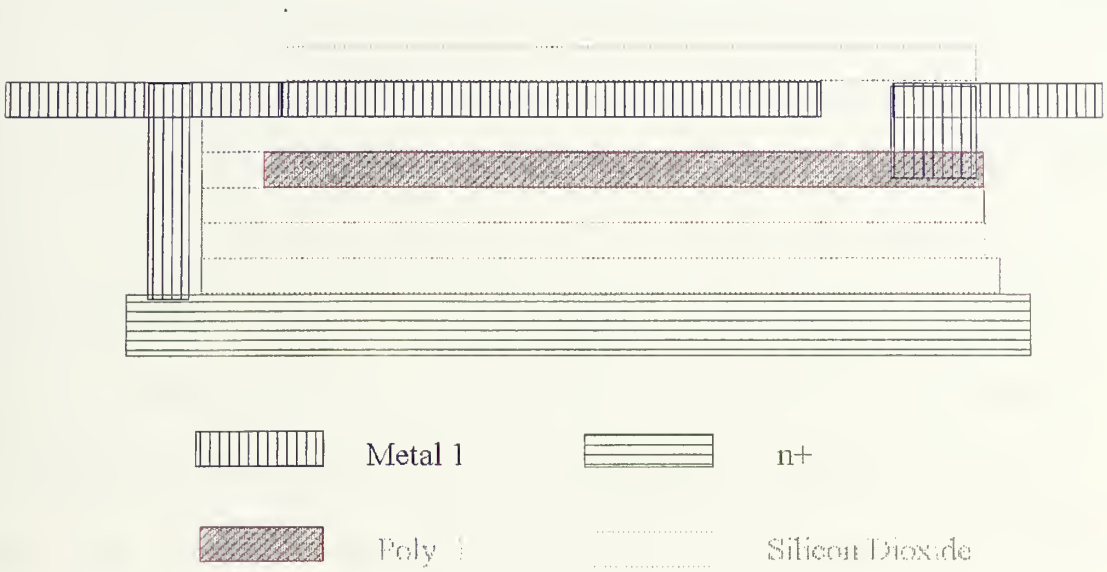


Figure A.8 The cross sectional view of the Cap_n+_poly2_metal1 capacitor.

APPENDIX B. EXPERIMENTAL DATA

This Appendix includes all the data recorded during the two days of testing. The first page is the data used to relate the charge on the SEM to total dose for both days. The second page contains the data used to relate total dose to capacitance for both days. The remaining data are the results from each individual chip test. The first chip does not contain the temperature data since it was not available. The time and the SEM charge (and temperature for the second chip) were the recorded results. The rest of the data is determined from the recorded data. Calculated data include; Total Time, Total Charge, Dose (determined from the SEM charge to dose relationships), Dose Rate, Total Dose, Fluence, Total Fluence. The other recorded data is the three dB downpoint which is used to determine the capacitance value. This data was not recorded at each time instance.

Data From the Dose to Charge Calibration (Both Days)

Charge (mV)	Dose (Rads)	Dose (Rads)	time (sec)	Dose Rate (Rads/sec)	Fluence (e/cm2)
	11/05/96	11/06/96			
100	634		17	37.29	4.0637E+11
150	742				6.0956E+11
150	789				6.0956E+11
120	574		19.9	28.84	4.8765E+11
100	518		14.6	35.48	4.0637E+11
80	324		15.1	21.46	3.2510E+11
60	345		9.2	37.5	2.4382E+11
60		978	9.5	102.95	2.4382E+11
50		823	7.4	111.22	2.0319E+11
46		832	4.5	184.89	1.8693E+11
40	304		4.5	67.56	1.6255E+11
30		478	2.7	177.04	1.2191E+11
23	98				9.3466E+10
20		326	2.2	148.18	8.1274E+10
10		99.4	2.9	34.28	4.0637E+10
0	0	0	0	0	0

average dose rate	average fluence
32.59	2.6389E+11

Data From the Capacitor vs Dose Plot

Time	Total Dose (Rads)	capacitor 1 (picofarads)	capacitor 2 (picofarads)
98	16.9	12.64	
102.7	15,925.4		13.72
289.6	49,430		14.76
686.1	39,820	14.03	
1,284.2	250,859		15.71
1,563.1	564,723	15.16	
1,831.1	911,341	15.68	
1,895.5	401,944		16.88
2,238.1	1,257,892	15.92	
2,621.1	603,399		17.55
3,346.1	804,854		17.74
3,966.1	1,006,309		17.7
4,827.1	1,610,724		18.77
5,960	2,399,779		19.41

Data From the Day One Run (5 November)

Time (sec)	Total time (sec)	Charge (V)	Total Charge (V)	Dose (Rads)	Dose Rate (Rads/sec)	Total Dose (Rads)	Fluence (e/cm2)	Total Fluence (e/cm2)	3 dB point (Hz)	Capacitor Value (picofarads)
98.9	98.9	0	0	16.93	0.17	16.93	0.0000E+00	0.0000E+00	12,590	12.64
10	108.9	0.1	0.1	511.93	51.19	528.86	4.0637E+11	4.0637E+11		
10.7	119.6	0.1	0.2	511.93	47.84	1,040.79	4.0637E+11	8.1274E+11		
13.4	133	0.1	0.3	511.93	38.2	1,552.72	4.0637E+11	1.2191E+12		
12.9	145.9	0.1	0.4	511.93	39.68	2,064.65	4.0637E+11	1.6255E+12		
12.9	158.8	0.1	0.5	511.93	39.68	2,576.58	4.0637E+11	2.0319E+12		
31.4	190.2	0.3	0.8	1,501.93	47.83	4,078.51	1.2191E+12	3.2510E+12		
31.4	221.6	0.3	1.1	1,501.93	47.83	5,580.44	1.2191E+12	4.4701E+12		
27.4	249	0.3	1.4	1,501.93	54.81	7,082.37	1.2191E+12	5.6892E+12		
28.2	277.2	0.3	1.7	1,501.93	53.26	8,584.3	1.2191E+12	6.9083E+12		
29.7	306.9	0.3	2	1,501.93	50.57	10,086.23	1.2191E+12	8.1274E+12		
190	496.9	3	5	14,866.93	78.25	24,953.16	1.2191E+13	2.0319E+13		
189.2	686.1	3	8	14,866.93	78.58	39,820.09	1.2191E+13	3.2510E+13	11,340	14.03
73	759.1	3	11	14,866.93	203.66	54,687.02	1.2191E+13	4.4701E+13		
54	813.1	3	14	14,866.93	275.31	69,553.95	1.2191E+13	5.6892E+13		
190	1,003.1	10	24	49,516.93	260.62	119,070.88	4.0637E+13	9.7529E+13		
120	1,123.1	10	34	49,516.93	412.64	168,587.81	4.0637E+13	1.3817E+14		
60	1,183.1	10	44	49,516.93	825.28	218,104.74	4.0637E+13	1.7880E+14		
55	1,238.1	10	54	49,516.93	900.31	267,621.67	4.0637E+13	2.1944E+14		
57	1,295.1	10	64	49,516.93	868.72	317,138.6	4.0637E+13	2.6008E+14		
55	1,350.1	10	74	49,516.93	900.31	366,655.53	4.0637E+13	3.0072E+14		
41	1,391.1	10	84	49,516.93	1,207.73	416,172.46	4.0637E+13	3.4135E+14		
64	1,455.1	10	94	49,516.93	773.7	465,689.39	4.0637E+13	3.8199E+14		
58	1,513.1	10	104	49,516.93	853.74	515,206.32	4.0637E+13	4.2263E+14		
50	1,563.1	10	114	49,516.93	990.34	564,723.25	4.0637E+13	4.6326E+14	10,500	15.16
40	1,603.1	10	124	49,516.93	1,237.92	614,240.18	4.0637E+13	5.0390E+14		
50	1,653.1	10	134	49,516.93	990.34	663,757.11	4.0637E+13	5.4454E+14		
32	1,685.1	10	144	49,516.93	1,547.4	713,274.04	4.0637E+13	5.8518E+14		
34	1,719.1	10	154	49,516.93	1,456.38	762,790.97	4.0637E+13	6.2581E+14		
35	1,754.1	10	164	49,516.93	1,414.77	812,307.9	4.0637E+13	6.6645E+14		

Time (sec)	Total time (sec)	Charge (V)	Total Charge (V)	Dose (Rads)	Dose Rate (Rads/sec)	Total Dose (Rads)	Fluence (e/cm2)	Total Fluence (e/cm2)	3 dB point (Hz)	Capacitor Value (picofarads)
37	1,791.1	10	174	49,516.93	1,338.3	861,824.83	4.0637E+13	7.0709E+14		
40	1,831.1	10	184	49,516.93	1,237.92	911,341.76	4.0637E+13	7.4772E+14	10,150	15.68
43	1,874.1	10	194	49,516.93	1,151.56	960,858.69	4.0637E+13	7.8836E+14		
184	2,058.1	30	224	148,516.93	807.16	1,109,375.62	1.2191E+14	9.1027E+14		
180	2,238.1	30	254	148,516.93	825.09	1,257,892.55	1.2191E+14	1.0322E+15	10,000	15.92
150	2,388.1	30	284	148,516.93	990.11	1,406,409.48	1.2191E+14	1.1541E+15		
86	2,474.1	30	314	148,516.93	1,726.94	1,554,926.41	1.2191E+14	1.2760E+15		
78	2,552.1	30	344	148,516.93	1,904.06	1,703,443.34	1.2191E+14	1.3979E+15		
80	2,632.1	13	357	64,366.93	804.59	1,767,810.27	5.2828E+13	1.4507E+15		
105	2,737.1	30	387	148,516.93	1,414.45	1,916,327.2	1.2191E+14	1.5727E+15		
120	2,857.1	30	417	148,516.93	1,237.64	2,064,844.13	1.2191E+14	1.6946E+15		
127	2,984.1	30	447	148,516.93	1,169.42	2,213,361.06	1.2191E+14	1.8165E+15		
120	3,104.1	30	477	148,516.93	1,237.64	2,361,877.99	1.2191E+14	1.9384E+15		
113	3,217.1	30	507	148,516.93	1,314.31	2,510,394.92	1.2191E+14	2.0603E+15		
126	3,343.1	30	537	148,516.93	1,178.71	2,658,911.85	1.2191E+14	2.1822E+15		
					Average Dose Rate (RADS/SEC) 0-813 sec	Average Dose Rate (RADS/SEC) 813-3343 sec				
					73.79	1,001.57				

Data From the Day Two Run (6 November)

Total time (sec)	Temp	Charge (V)	Total Charge (V)	Dose (Rads)	Dose Rate (Rads/sec)	Total Dose (Rads)	Fluence (e/cm2)	Total Fluence (e/cm2)	3 dB point (Hz)	Capacitor Value (picofarads)
102.7	49.2	0.95	0.95	15,925.4	155.07	15,925.4	3.8605E+12	3.8605E+12	11,600	13.72
162.7	50.4	0.5	1.45	8,369.9	139.5	24,295.3	2.0319E+12	5.8924E+12		
204.9	51.5	0.5	1.95	8,369.9	198.34	32,665.2	2.0319E+12	7.9243E+12		
289.6	53.5	1	2.95	16,764.9	197.93	49,430.1	4.0637E+12	1.1988E+13	10,780	14.76
778.6	57.7	6	8.95	100,714.9	205.96	150,145	2.4382E+13	3.6370E+13		
1,284.2	54.8	6	14.95	100,714.9	199.2	250,859.9	2.4382E+13	6.0753E+13	10,129	15.71
1,895.5	53.5	9	23.95	151,084.9	247.15	401,944.8	3.6573E+13	9.7326E+13	9,430	16.88
2,621.1	51.7	12	35.95	201,454.9	277.64	603,399.7	4.8765E+13	1.4609E+14	9,070	17.55
3,346.1	49.9	12	47.95	201,454.9	277.87	804,854.6	4.8765E+13	1.9486E+14	8,970	17.74
3,966.1	49.8	12	59.95	201,454.9	324.93	1,006,309.5	4.8765E+13	2.4362E+14	8,990	17.7
4,827.1	50.7	36	95.95	604,414.9	701.99	1,610,724.4	1.4629E+14	3.8991E+14	8,480	18.77
5,602.2	49.2	36	131.95	604,414.9	779.79	2,215,139.3	1.4629E+14	5.3621E+14		
5,705		4	135.95	67,134.9	653.06	2,282,274.2	1.6255E+13	5.5246E+14		
5,960	49.7	7	142.95	117,504.9	460.8	2,399,779.1	2.8446E+13	5.8091E+14	8,199	19.41
					Average Dose Rate (RADS/SEC)					
					344.23					

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